digital EQUIPMENT CORPORATION MAYNARD MASSACHUSETTS

DRAWING DIRECTORY

CUSTOMER PRINT SET INDEX

THIS IS PRINT SET [X]

SEQUENCE		SEQUENCE	
DRAWING DIRECTORY	B-DD-AR11-Ø		
ANALOG REALTIME SUBSYSTEM	A-PL-AR11-Ø-Ø		
ACCESSORY LIST	A-AL-AR11-Ø-1		
**WRAP AROUND MAINT. KIT	A-PL-BG5Ø36-Ø-Ø		
AR11	D-CS-M78Ø9-Ø-1		
WRAP AROUND MODULE	D-CS-G5Ø36-Ø-1		
**CABLE, BC11L	D-UA-BC11L-Ø-Ø		
SYS. INSTALL./ACCEPT.	A-SP-AR11-Ø-4		
CIRCUIT DESCRIPTIONS	A-SP-AR11-Ø-5		
TROUBLE SHOOTING INFO.	A-SP-AR11-Ø-6		
MULTI-LAYER REWORK STD.	A-SP-7665169-0-0		

UNIT VARIATIONS

VAR	TITLE	PRINT SET AR11
AR11-Ø	ANALOG REALTIME SUBSYSTEM	X

**INDICATES OPTION

REVISIONS	REV	CHG. NO.	DATE

USED ON OPTION/MODEL

SHEET 1 OF 2

DRN. D. K. CRABBE	DATE 8/30/74	TITLE: ANALOG REALTIME SUBSYSTEM
CHK'D. DK Cobb	DATE 9-9-74	
PROJ ENG. Jesse Orsecan	DATE 9/9/74	
PROD. [illegible]	DATE 9/10/74	SIZE B · CODE DD · NUMBER AR11-Ø · REV
FIELD SERV. [illegible]	DATE 9/9/74	DIST

DEC 16-13251-1043-1A-N92

DDB 106

ELECTRICAL

CUSTOMER PRINT SET: AR11	MFG. SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE
X		1	A-PL-AR11-Ø-Ø	-	1	ANALOG REALTIME SUBSYSTEM	
X			D-CS-M78Ø9-Ø-1		16	AR11	
X			D-CS-G5Ø36-Ø-1		2	WRAP AROUND MODULE	
X			A-AL-AR11-Ø-1		1	ACCESSORY LIST	
	X		A-SP-AR11-Ø-2		*	ENGINEERING SPEC.	
	X		A-SP-AR11-Ø-3		*	OPTION CHECKOUT/ACCEPT.	
X			A-SP-AR11-Ø-4		*	SYS. INSTALL./ACCEPT.	
X			A-SP-AR11-Ø-5		*	CIRCUIT DESCRIPTIONS	
X			A-SP-AR11-Ø-6		*	TROUBLESHOOTING INFO.	
X			A-SP-7665169-0-0		*	MULTI-LAYER REWORK STD.	
X		**	D-UA-BC11L-Ø-Ø		1	CABLE, BC11L	
X		**	A-PL-BG5036-Ø-Ø		1	WRAP AROUND MAINT. KIT	
	X		B-DD-AR11-TA	-	1	CHECKOUT TESTER	
	X		B-DD-AR11-TB	-	1	BURNIN SYSTEM	
		**	INDICATES OPTION				

CUSTOMER PRINT SET	MFG SET	FIND NO.	DRAWING NO.	REV	NO OF SHT	DESCRIPTION	OPTION NO./FILE DATE

CUSTOMER PRINT SET CODES

X = PRINT OF DOCUMENT INCLUDED IN PRINT SET
C = INCLUDES ALL PRINTS INDICATED ON DOCUMENT
S = CONFIDENTIAL AUTHORIZED SIGNATURE REQUIRED

TITLE	SHEET	SIZE	CODE	NUMBER	REV
ANALOG REALTIME SUBSYSTEM	2 OF 2	B	DD	AR11-Ø	

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

MADE BY D.K.Crabbe DATE 8-19-74	CHECKED D.K. Crabbe DATE 8-27-74	SECTION 1
ENG Jess Lipcon DATE 8-26-74	PROD F.W. Cutting DATE 9-10-74	ISSUED SECT. 1

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION AR11-Ø
1	D-CS-M78Ø9-Ø-1	AR11	1
2	1210089-4	Pins, Mating Socket	60
3	1210918-15	Housing, Mating Berg	1
4	1700021-0	Shield, 7 1/2 X 15 3/8	2

TITLE Analog Real-time Subsystem	ASSY NO B-DD-AR11-Ø	SIZE A	CODE PL	NUMBER AR11-Ø-Ø	REV / ECO NO
	SHEET 1 OF 1	DIST			

DEC FORM DEC 16-(325)-1031-N870
DRA 110

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ACCESSORY LIST

MADE BY D.K.Crabbe	CHECKED RRCatlett	SECTION 1
DATE 8-19-74	DATE 8-27-74	
ENG Jesse Lipcon	PROD J.P.Curtin	ISSUED SECT. 1
DATE 8-26-74	DATE 9-10-74	

LEGEND

D DOCUMENT
DN DOCUMENT CHANGE NOTICE
PA PAPER TAPE ASCII
PB PAPER TAPE BINARY
PM PAPER TAPE READ-IN-MODE

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION AR11	KIT CHECK BY ____ DATE ____	INSTALLATION CHECK BY ____ DATE ____
1	B-DD-AR11-Ø	Drawing Directory	1		
2	1210089-4	Pins, Mating Socket	60		
3	1210918-15	Housing, Mating Berg	1		
4	DEC-11-HARUG-A-D	User's Manual	1		
5	MAINDEC-11-DZARA-A	AR11 Diagnostic Test I (Logic)	1		
6	MAINDEC-11-DZARB-A	AR11 Diagnostic Test II (Analog)	1		
7	MAINDEC-11-DZARC-A	AR11 Wraparound Diagnostic	1		
8	MAINDEC-11-DXARA-A	AR11 DECX-11 Exerciser Module	1		

TITLE Accessory List AR11	ASSY. NO. B-DD-AR11-Ø	SIZE A	CODE AL	NUMBER AR11-Ø-1	REV.	ECO NO
	SHEET 1 OF 1	DIST				

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

PARTS LIST

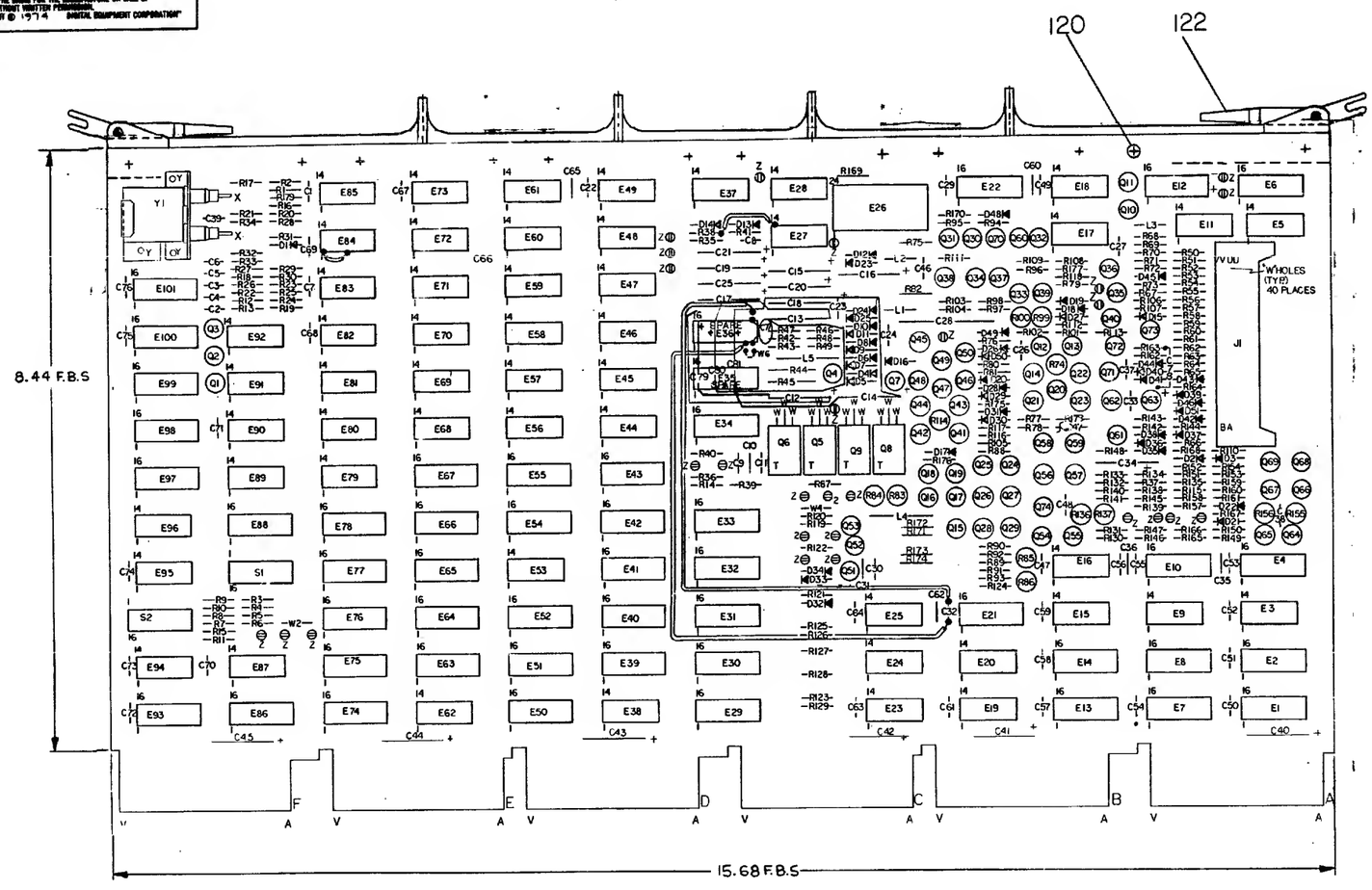
MADE BY D.K.Crabbe	CHECKED	SECTION 1
DATE 8-19-74	DATE	
ENG Jesse Lipcon	PROD	ISSUED SECT. 1
DATE 8-26-74	DATE 9-10-74	

ITEM NO.	DWG NO./PART NO.	DESCRIPTION	QUANTITY/VARIATION BG5Ø36-Ø
1	D-CS-G5Ø36-Ø-1	Wraparound Module	1
2	D-UA-BCØ8R-Ø6-Ø	BCØ8R I/O Cable	1

TITLE Wraparound Maintenance Kit	ASSY NO. B-DD-AR11-Ø	SIZE A	CODE PL	NUMBER BG5Ø36-Ø-Ø	REV.	ECO NO.
	SHEET 1 OF 1	DIST				

DEC FORM DEC 16-(325)-1031-N870

NOTES:



AA2, BA2, CA2, DA2, EA2, FA2 — +5V
C40 THRU C45 15 µf
C50 THRU C76 .01µf
AC2, AT1, BC2, BT1, CC2, DC2, ET1, FC2, FT1

REF				
REF		X-Y COORDINATE HOLE LOCATION	K-CS-M7809-0-4	1
REF		ASSY/DRILLING HOLE LAYOUT	D-AH-M7809-0-5	2
REF		MODULE ECO HISTORY	9-MH-M7809-0-6	3
1		ETCHED CIRCUIT BOARD	5010078	4
1	C1	CAP 470 PF 100V 5% DM	1000024	5
5	C2,C3,C4,C11,C32	CAP 560 PF 100V 5% DM	1000025	6
2	C5,C6	CAP 5000 PF 100V 20% DISC	1001785	7
1	C7	CAP 1500 PF 250V 10% DISC	1000064	8
2	C8,C10	CAP 220 PF 100V 5% DM	1000021	9
1	C9	CAP 270 PF 100V 5% DM	1000022	10
6	C12,C13,C14,79,80,81	CAP 30 UF 10V 10% S TANT	1000078	11
16	C15 THRU C21,C25,C34, C40 THRU C45,C78	CAP 15 UF 20V 10% S TANT	1004812	12
1	C22	CAP 680 PF 100V 5% DM	1000028	13
36	C48 THRU C76,C23,C24,C28, C30,C35	CAP .01UF 100V DISC	1001616-81	14
2	C27,C39	CAP 100 PF 100V 5% DM	1000015	15
1	C29	CAP .001 UF 100V 10% PST	1000036	16
3	C29,C38,C38	CAP 27 PF 100V 5% DM	1001736	17
1	C31	CAP 3300 PF 50V 6% CER	1011676	18
3	C33,C37,C77	CAP 1000 PF 250V 20% DISC	1000043	19
1	D20	DIODE-MCL 1301 1MA	1105618	20
1	D47	DIODE IN 4732 A 4.7V	1105138	21
43	D2 THRU D12,D15 THRU D19, D21 THRU D30;D33 THRU D46, D46,D50,D51	DIODE D672	1105275	22
1	D14	DIODE IN 756 A 0.2V	1103441	23
1	D49	DIODE IN 825 6.2 V	1101385	24
1	D31	DIODE IN 751 A 5.1V	1110094	25
2	D1,D32	DIODE IN 748 A 3.3V	1104880	26
1	D13	DIODE IN 754 A 8.0V	1100001	27
2	S1,S2	SW PACK	1211184-4	28
2		COVER (SW PK)	1211284-4	29
1	J1	BERG CONN.	1209941	30
2	R99,R100	RES200Ω¼W 10% 62 PR POT	1300156-10	31
3	R85,R86,R114	RES 2K ¼W 10% 62 PR POT	1300160-7	32
7	R74,R83,R84,136,137 155,156	RES 500 ¼W 10% 62 PR POT	1300158-8	33
39	R1,R11,R14,R15,R28,R31, R34,R35,R38,R40 THRU R43,R49,R88,R90,R103, R104,R112,R113,R115, R118,R108,R118,R123,R129, R142,R143,R146,R147,R162, R163,R165,R166,R168,R170, R176,R117,R128	RES 1.1K ¼W 5%	1301475	34
3	R12,R13,R46	RES 270 ¼W 5%	1301972	35
3	R2,R107,R179	RES 100 ¼W 5%	1300220	36
4	R18,R22,R23,R26	RES 390 ¼W 5%	1300309	37
4	R17,R21,R24,R25	RES 180 ¼W 5%	1301322	38
1	R28	RES 470 ¼W 5%	1300316	39
1	R30	RES 330 ¼W 5%	1300285	40
12	R32,R33,R120,R124,R3 THRU R10	RES 10K ¼W 5%	1300479	41
3	R38,R177,R96	RES 4.7K ¼W 5%	1300447	42
3	R37,R48,R125	RES 3.3K ¼W 5%	1300430	43
1	R39	RES 47K ¼W 5%	1302177	44
2	R44,R45	RES 82 ¼W 5%	1301781	45
1	R47	RES 150 ¼W 5%	1300250	46
QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

FIRST USED ON OPTION MODEL

PARTS LIST

ETCH BOARD REV. C

IC TYPE	GND	+5V
GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE		
IC PIN LOCATIONS		

REV.	REVISIONS	CHANGE NO.	CHK	DATE
A	ORIGINATED	M7809-00001	J. Lipcon	13 OCT 76
B		M7809-00002	J. Lipcon	14 SEPT 76
C		M7809-00003	J. Lipcon	3-3-75
D		M7809-00004	J. Lipcon	12-5-74
E			J. Lipcon	3-3-75

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN. E. Beasley	DATE 7-23-74	digital
CHKD. J. Fagan	DATE 8-27-74	
ENG. Jose Lopez	DATE 8-22-74	TITLE AR11
PROJ. ENG. Jose Lopez	DATE 8-22-74	
PROD. [illegible]	DATE [illegible]	
NEXT HIGHER ASSY		SIZE D CODE CS NUMBER M7809-0-1 REV. E
SCALE NONE		DIST.
SHEET 1 OF 16		

M7809-0-1 E
DCS

NOTES:

3	E15,E18,E92	IC DEC 7410	1909928	96	3	R144,R164,R180	RES 47 1/4W 1% FUSIBLE	1310881-2	47
7	E17,E73,E83,E84,E85,E95,E96	IC DEC 8881	1908705	97	3	R97,R98,R175	RES 7.5K 1/4W 5%	1301422	48
4	E50,E51,E52,E07	IC DEC 8641 (8838)	1911117	98	12	R87,THRU R72,R88,R122,R132,R133,R153,R154	RES 20K 1/4W 5%	1302391	49
7	E10,E24,E30,E40,E57,E89,E01	IC DEC 7402	1909004	99	2	R73,R178	RES 100K 1/4W 5%	1302468	50
					3	R75,R171,R172	RES 1.09K 1/8W .1% 25 PPM/°C	1309297	51
11	E20,THRU E33,E42,E54,E86,E78,E88,E07	IC DEC 74151	1909936	100	10	R50 THRU R85	RES 1K 1/4W 1% FUSIBLE	1310881-0	52
					2	R76,R105	RES 750 1/4W 5%	1301401	53
1	E56	IC DEC 74157	1910355	101	4	R77,R79,R126,R86	RES 2K 1/4W 5%	1302368	54
8	E23,E25,E44,E45,E58,E58,EWO,E01,E78	IC DEC 7474	1905547	102	1	R78	RES 810 1/4W 5%	1305374	55
1	E71	IC DEC 7408	1910155	103	3	R81,R101,R102	RES 1.2K 1/4W .5% 25 PPM/°C	1301880	56
1	E02	IC DEC 7427	1910070	104	1	R82/	RES 1.0K 1/4W .1% 25 PPM/°C	1309295	57
1	E37	IC DEC 7420	1905577	105	2	R87,R121	RES 3K 1/4W 5%	1300432	58
4	E00,E00,E100,E101	IC DEC 74100	1910095	106					
2	E40,E41	IC DEC 74193	1910010	107	1	R89	RES 2.2K 1/4W 5%	1300417	59
10	E1,E7,E13,E14,E30,E04,E05,E75,E70,E77	IC DEC 74175	1910051	108	1	R91	RES 500 1/4W 5%	1301090	60
					2	R92,R93	RES 5.8K 1/4W 5%	1301074	61
1	E60	IC DEC 7451	1905020	109	6	R94,95,130,131,149,150	RES 2.7K 1/4W 5%	1300426	62
1	E20	IC AM 2504	1911020	110	1	R106	RES 33 1/4W 5%	1300197	63
2	E21,E34	IC DEC 74123	1910439	111	2	R109,R111	RES 382 1/4W .1% 25 PPM/°C	1300201	64
2	E16,E47	IC DEC 7405	1908930	112	2	R110,R118	RES 15K 1/4W 5%	1300496	W5
1	E27	IC DEC 7400	1910741	113	1	R127	RES 80 1/4W 5%	1300219	66
1	E49	IC DEC 7403	1909054	114	2	R134,R151	RES 422 1/4W 1% 25 PPM/°C	1300314	W7
2	E0,E12	IC OG 501C (AM3705C,IM7118C)	1911598	115	2	R135,R152	RES 464 1/4W 1% 100 PPM/°C	1303047	68
3	E4,E19,E22	IC MC 1400L8	1811029	116	4	R136,R138,R157,R159	RES 3K 1/8W .1% 25 PPM/°C	1302876	69
1	E29	IC DEC 7453	1905502	117	2	R140,R158	RES 1.882K 1/4W .1% 25 PPM/°C	1302877	70
4	E2,E0,E43,E63	IC DEC 74174	1910852	118	2	R141,R100	RES 1.21K 1/8W 1% 50 PPM/°C	1302741	71
2	E5,E11	DIODE PK 2501-01	1910010-01	118	2	R19,R27	RES 383 1/8W 1% 100 PPM/°C	1305125	72
12		EYELETS FOR HANDLE	9006732	120	2	R16,R20	RES 178 1/8W 1% 100 PPM/°C	1311422	73
27		SPLIT LUGS	9008735	121	2	R145,R181	RES 798 1/8W 1% 25 PPM/°C	1309292	74
1		HANDLE (MEX)	1210711	122	2	R148,R167	RES 3.987 1/8W 1% 25 PPM/°C	1302878	75
2		CRYSTAL SOCKET	1202812	123	2	R173,R174	RES 9.09K 1/8W 1% 25 PPM/°C	1305430	76
1		CRYSTAL HOLDER BRKT.	5303154	124	2	Q60,Q70	FET 2N5460	1510233	77
1		REAR SUPPORT BRKT.	5302825	125	4	Q1,Q2,Q3,Q5?	TRANSISTOR 3009B	1503100	78
2	W2,W4	INSULATED JUMPER	8009185	126	2	Q5,Q8	TRANSISTOR 045C8	1510414	79
3		SCREWS FOR BRKT. (PAN HEAD)	9009001-1	127	2	Q6,Q9	TRANSISTOR 044C3	1510171	80
3		HEX NUTS (2-56)	9009555	128	11	Q4,Q7,Q10,Q30,Q31,Q32,Q52,Q54,Q55,Q64,Q65	TRANSISTOR 65340	1503409	81
A/R		WIRE, 30 AWG	9105740	129	3	Q11,Q48,Q49	FET 2N5245	1509801	02
3		WASHER INT. TOOTH	9006631	130	34	Q12 THRU Q19,Q21,Q22,Q24 THRU Q29,Q33 THRU Q36,Q41 THRU Q45,Q58,Q57,Q61,Q62,Q66,Q67,Q71,Q72,Q74	TRANSISTOR 2N4250	1509142	03
1	E90	IC DEC 380	1912549	131	16	Q20,Q23,Q37 THRU Q40,Q48,Q47,Q53,Q58,Q63,Q68,Q69,Q73,Q58,Q59	TRANSISTOR SE4020	1509567	04
					3	L1,L2,L3	INDUCTOR 100 UH	1810682	05
					2	L4,L5	INDUCTOR .22 UH	1003377	06
					1	Y1	CRYSTAL 1 MHZ	1005501-1	07
					2	E96,E93	IC DEC 9937	1911116	09
					2	E87,E94	IC DEC 9242	1909712	09
					1	E74	IC DEC 9251 B	1909594	90
					1	E62	IC DEC 314	1909704	91
					2	E89,E91	IC DEC 384	1909488	92
					1	E80	IC DEC 8640 (380)	1909405	93
					4	E28,E53,E56,E72	IC DEC 7400	1905575	94
					4	E3,E9,E48,E79	IC DEC 7404	1909006	95
					QTY	REF. DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

PARTS LIST

DEC 74174	8	16
DEC 7493	10	5
DEC 74123	8	16
AM 2504	12	24
DEC 74175	8	16
DEC 74193	8	16
DEC 74190	8	16
DEC 74157	8	16
DEC 74151	8	16
DEC 8641 (8838)	8	16
DEC 8640 (380)	1	8
DEC 384	1	8
DEC 314	1	8
DEC 8251 B	8	16
DEC 8837	8	16
IC TYPE	GND	+5V

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

FIRST USED ON OPTION MODEL

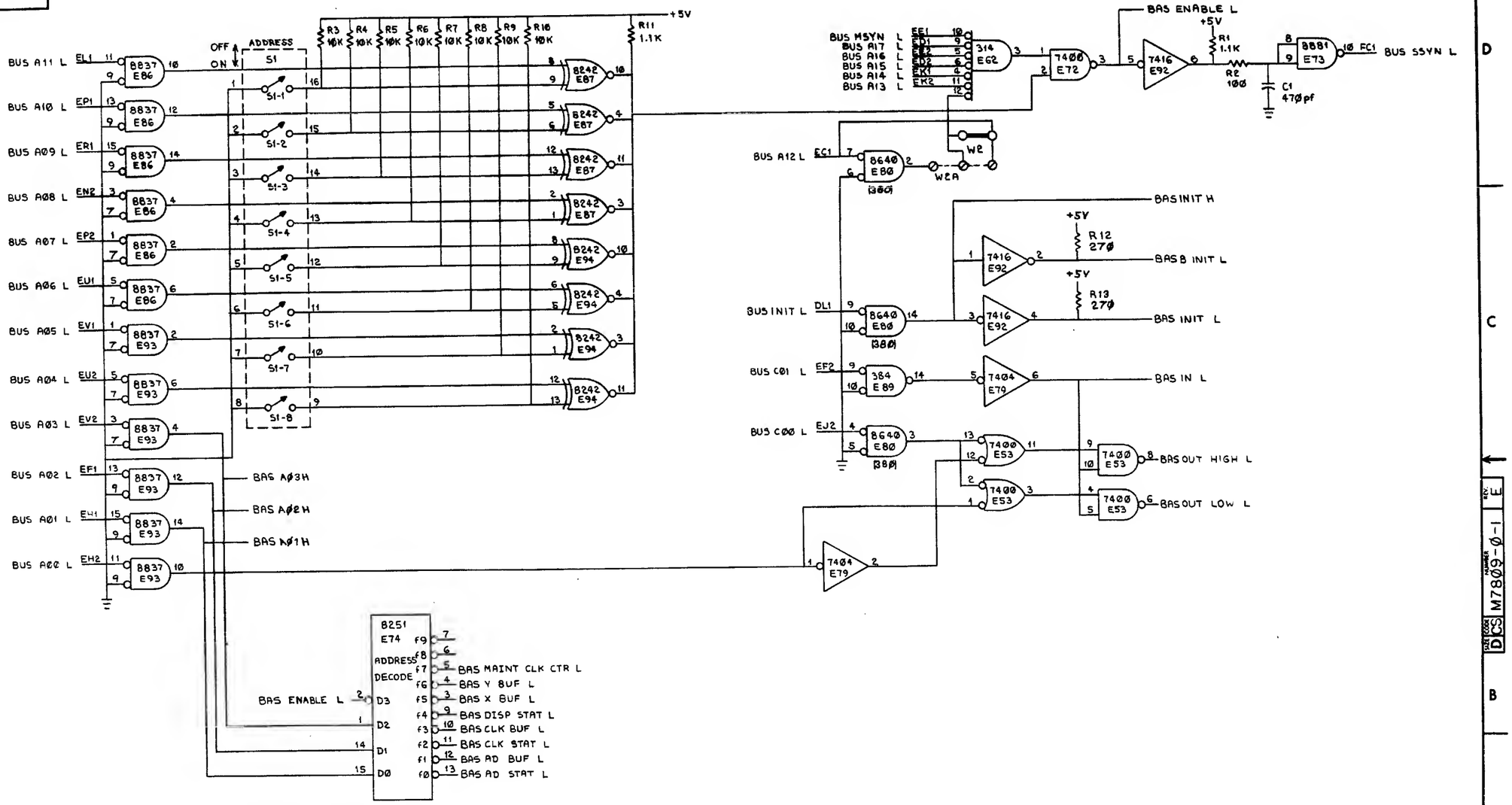
ORIGINATED	A
CHK	CHANGE NO.
	REVISIONS

DEC NO.	EIA NO.	DEC NO.	EIA NO.

SEMICONDUCTOR CONVERSION CHART

DRN. P. Beasley	DATE 5/12/74	digital
CHK'D. [illegible]	DATE 5-15-74	TITLE AR11
ENG. [illegible]	DATE 5-22-74	
PROJ. ENGR. [illegible]	DATE 5-22-74	
PROD. [illegible]	DATE 5-23-74	
NEXT HIGHER ASSY		SIZE D CODE CS NUMBER M7809-0-1 REV. E
SCALE NONE		DIST.
SHEET 2 OF 16		

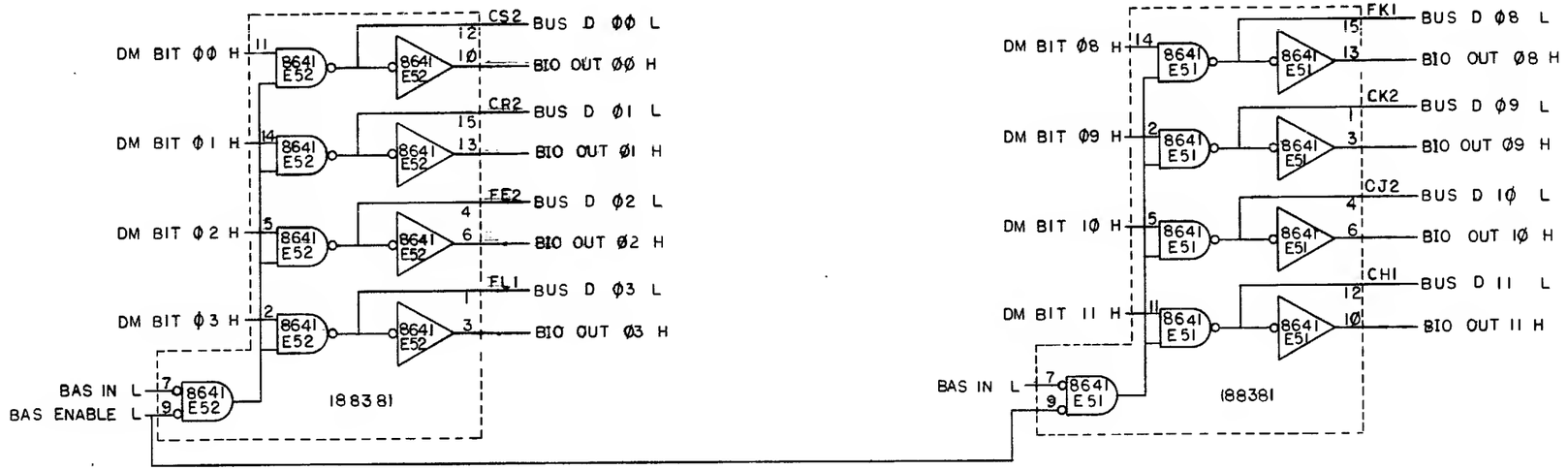
REV. E | SIZE D | CODE CS | NUMBER M7809-0-1

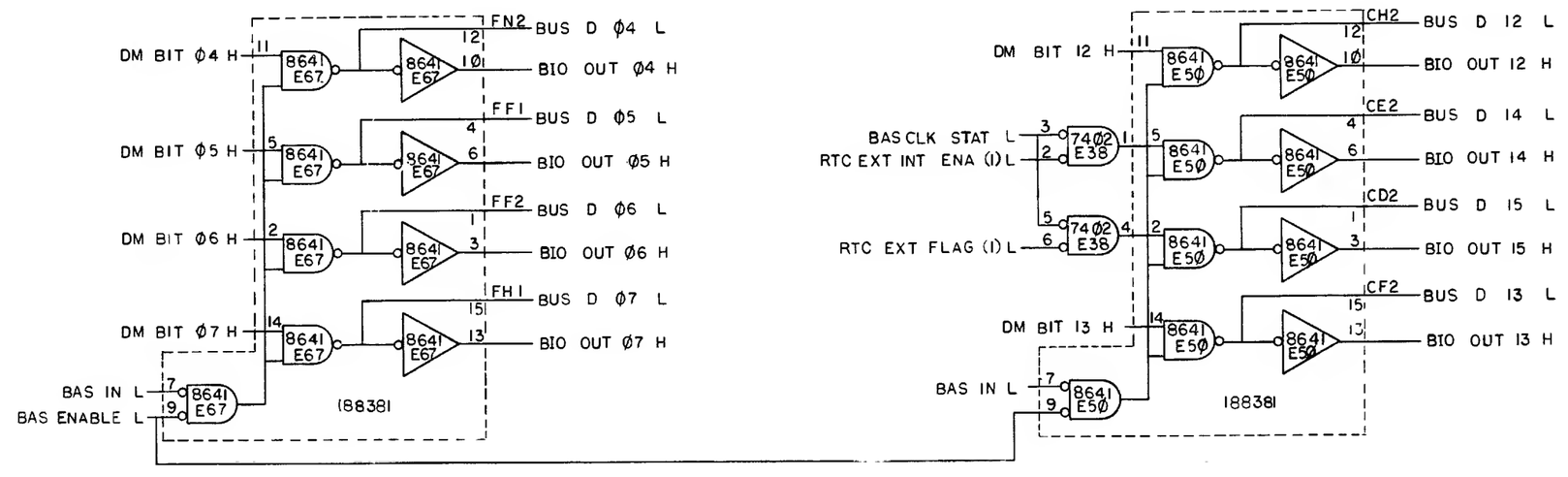


BAS (BUS ADDRESS SELECT)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
AR II	D	CS	M7809-0-1	E
SCALE NONE	SHEET 3 OF 16		DIST.	



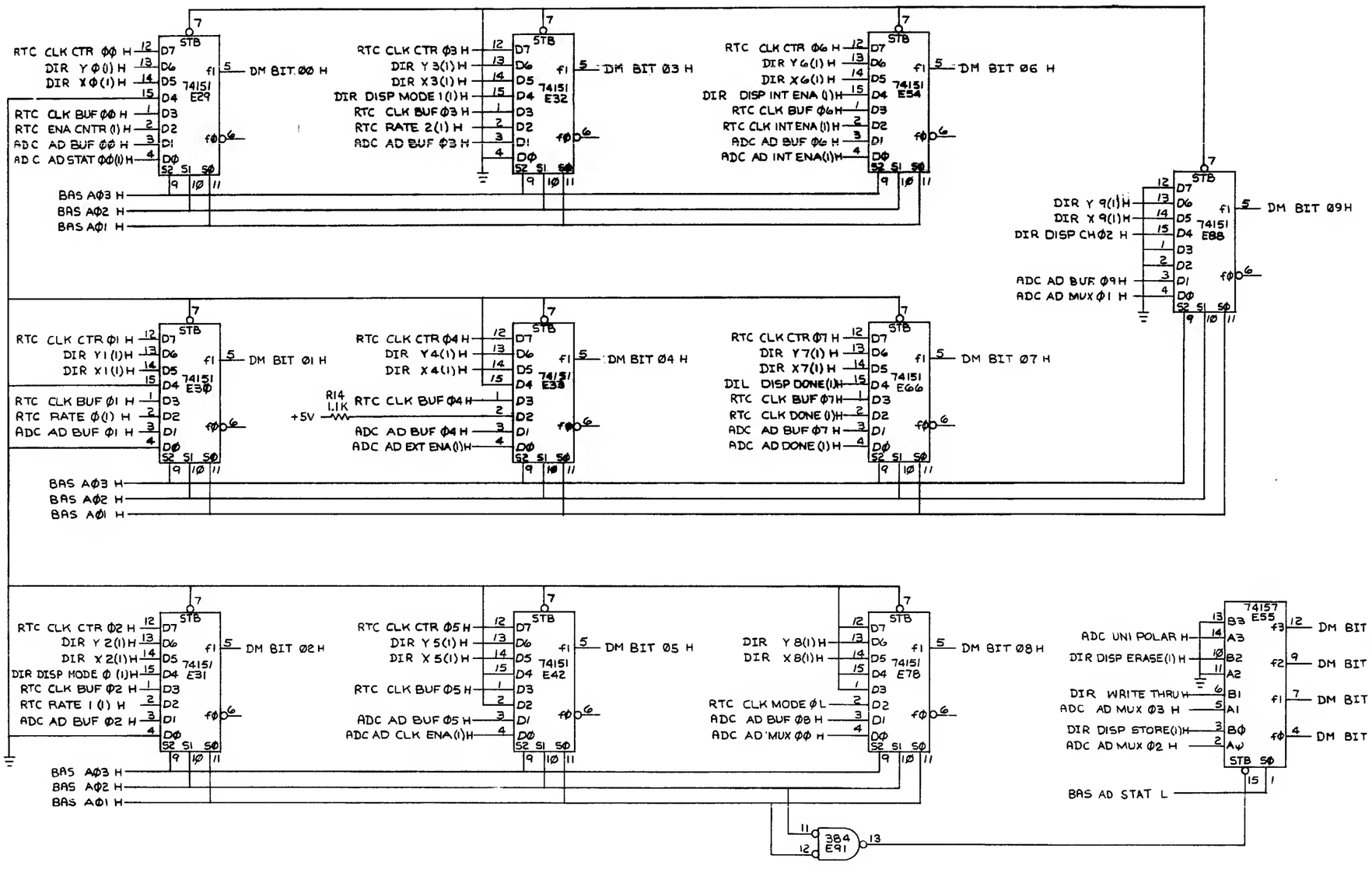


REVISIONS		
CHK	CHANGE NO.	REV.

BIO (BUS IN/OUT)

TITLE	SIZE	CODE	NUMBER	REV.
AR11	D	CS	M7809-Ø-1	E
SCALE NONE	SHEET 4 OF 16	DIST.		

M7809-Ø-1 E
DCS



REVISIONS		
CHK	CHANGE NO.	REV.

DM (DATA IN MULTIPLEXERS)

TITLE	SIZE	CODE	NUMBER	REV.
AR II	D	CS	M7809-Ø-1	E
SCALE NONE	SHEET 5 OF 16		DIST.	

DEC FORM NO DRD 1...

RTC +3V
IV FF1A (1) H
7474 FF1A E89
8881 E84
4 DE2
BR 6 L
ADC INT A H
BAS INIT L
7408 E71
BG 6 IN H
DM2
384 E91
A27 383
+5V
7416 E92
R26 390
Q3 3009B
8881 E83
R24 180
R25 180
C4 560pf
IV GO L
IV FF2A(Ø) L
7427 E82
RTC +3V
IV FF1B (1) H
7474 FF1B E69
8881 E84
DE2
BR 6 L
RTC INT B H
7408 E71
IV BG 6 PASS
R23 390
384 E91
+5V
7416 E92
R22 390
Q2 3009B
8881 E85
R20 178
R21 180
C3 560pf
IV FF2B(Ø) L
IV GO L
7427 E82
RTC +3V
7474 FF1C E61
8881 E73
4 DH2
BR 4 L
DIL INT C H
7408 E71
+5V
7416 E92
R18 390
Q1 3009B
8881 E85
R16 178
R17 180
C2 560pf
BG 4 IN H
DS2
384 E91
R19 383
IV FF2C(Ø) L
IV GO L
7427 E82

7400 E72
8881 E83
FD1 BUS BBSY L
FT2 BUS SACK L
IV FF2A(Ø) L
IV BG 6 PASS
IV FF1A(1) H
7474 FF2A E59
7400 E72
8881 E84
FD1 BUS BBSY L
FT2 BUS SACK L
IV FF2B(Ø) L
DN2 BG 6 OUT H
IV FF1B(1) H
7474 FF2B E69
8881 E73
FT2 BUS SACK L
FD1 BUS BBSY L
IV MASTER C H
8640 E80
(38Ø)
DT2 BG 4 OUT H
IV FF 2C (Ø) L
7474 FF2C E61
8881 E85

IV MASTER C L
7420 E37
IV MASTER C H
7404 E79
IV MASTER C L
BUS SSYN L
FCI
384 E89
384 E89
7402 E38
IV A INT DONE L
7402 E38
IV B INT DONE H
7402 E38
IV DISP INT DONE H
384 E89
7400 E72
IV GO L

VECTOR
+5V
R1Ø 1.1K
OFF
ON
S2-1
S2-2
S2-3
S2-4
S2-5
8881 E95
8881 E95
8881 E95
8881 E95
8881 E96
8881 E96
8881 E96
8881 E96
FK1 BUS DØ8 L
FH1 BUS DØ7 L
FF2 BUS DØ6 L
FF1 BUS DØ5 L
FN2 BUS DØ4 L
FM BUS INTR L
FL1 BUS DØ3 L
FE2 BUS DØ2 L

BG5 IN H DP2 — DR2 BG5 OUT H
BG7 IN H DK2 — DL2 BG7 OUT H

REVISIONS		
CHK	CHANGE NO.	REV.

IV (INTERRUPTS AND VECTORS)

TITLE	SIZE	CODE	NUMBER	REV.
AR11	D	CS	M7809-Ø-1	E
SCALE NONE	SHEET 6 OF 16		DIST.	

BAS B INITL
RTC TEST COUNTER H
RTC ENA CNTR (1) L
TPC Ø
RTC PS CLK
5000 PF C5
10K R32
10K R33
R179 180
Y1 1MHZ CRYSTAL
5000 PF C6
100PF C39
1.1K R34
RTC 1MHZ L
RTC 100 KHZ L
RTC 10 KHZ L
RTC 1 KHZ L
RTC 100 HZ L
BAS INIT L
RTC CLK OVR FLW L
RTC CLK OVRFLW H
ADC EXT ST (1) L
BIO OUT 15 H
RTC EXT FLAG (1) L
BAS B INIT L
RTC EXT INT ENA (1) H
RTC EXT INT ENA (1) L
RTC TEST COUNTER H
RTC CLK MODE Ø L
RTC CLK MODE 1 L
RTC +3V
AUX CLK L
+5V
RTC RATE Ø (1) H
RTC RATE 1 (1) H
RTC RATE 2 (1) H
BAS MAINT CLK CTR L
RTC CLK OUT L
BIO OUT ØT H
BIO OUT Ø6 H
BIO OUT Ø5 H
BIO OUT Ø4 H
RTC CLK BUF ØT H
RTC CLK BUF Ø6 H
RTC CLK BUF Ø5 H
RTC CLK BUF Ø4 H
RTC CLK CTR ØT H
RTC CLK CTR Ø6 H
RTC CLK CTR Ø5 H
RTC CLK CTR Ø4 H
BIO OUT 14 H
BIO OUT 11 H
BIO OUT 8 H
BAS INIT H
RTC LD CLK CNTR L
BIO OUT Ø3 H
BIO OUT Ø2 H
BIO OUT Ø1 H
BIO OUT ØØ H
RTC CLK BUF Ø3 H
RTC CLK BUF Ø2 H
RTC CLK BUF Ø1 H
RTC CLK BUF ØØ H
RTC CLK CTR Ø3 H
RTC CLK CTR Ø2 H
RTC CLK CTR Ø1 H
RTC CLK CTR ØØ H
BIO OUT 03 H
BIO OUT 02 H
BIO OUT 06 H
BIO OUT Ø1 H
RTC RATE 2 (1) H
RTC RATE 1 (1) H
RTC RATE Ø (1) H
RTC CLK INT ENA (1) H
RTC CLK OVRFLW H
ADC EXT ST (1) H
RTC LD CLK LOW H
RTC INT B H
RTC + 3V
IV B INT DONE H
BAS INIT H
BIO OUT ØØ H
RTC LD CLK LOW H
RTC ENA CNTR (1) H
RTC ENA CNTR (1) L
RTC ENA CNTR (Ø) H
RTC CLK MODE Ø L
RTC CLK OVRFLW L
BIO OUT ØT H
RTC CLK DONE (1) H
BAS INIT L
BAS CLK BUF L
BAS OUT LOW L
RTC ENA CNTR (Ø) H
RTC LD CLK CNTR L
BAS OUT HIGH L
BAS CLK STAT L
BAS OUT LOW L
RTC CLK MODE 1 L
RTCCLK OVRFLW L
1500 PF C7
330 R30
470 R29
3.3V 1N746A D1
+5V

REVISIONS		
CHK	CHANGE NO.	REV.

RTC (RT CLOCK LOGIC)

TITLE	SIZE	CODE	NUMBER	REV.
AR II	D	DCS	M7809-0-1	E
SCALE NONE	SHEET 7 OF 16	DIST.		

R41 1.1K +5V

7493 E49 — R3(1), R2(1), R1(1), R0(1), CLR, CLK0, CLK1

7404 E48 — 7420 E37 — 7474 E45 — 7400 E56 — 7400 E56 — 680 PF C22

RTC PS CLK

HQP AD CLK H

7406 E27 — HQP A L

7406 E27 — HQP B L

7406 E27 — 7406 E27 — 7406 E27 — HQP C L

7406 E27

+5V R42 1.1K — Q4 6534D — L4 .22µH

R43 1.1K — R44 82½W — Q5 D45C6 — HQP A L

TP PD — *C81 39µF — HQP B L — C14 39µF

*C79 39µF — C12 39µF

D4 D672 — D6 D672 — D8 D672

D5 D672 — D7 D672 — D9 D672

R49 1.1K — R48 3.3K — R47 150 — Q7 6534D — Q8 D45C6

R45 82½W — HQP C L — Q6 D44C3 — L5 .22µH

C13 39µF — *C80 39µF

R46 270 — Q9 D44C3

D14 IN756A 8.2V — D13 IN754A 6.8V

C20 15µF — C18 15µF — D23 D672 — D24 D672 — L2 100µH — TP-

D12 D672 — D25 D672 — -14V HQ

C17 15µF — C19 15µF — C25 15µF — C24 .01µF

+5V — TP HQ — HQ GND

C15 15µF

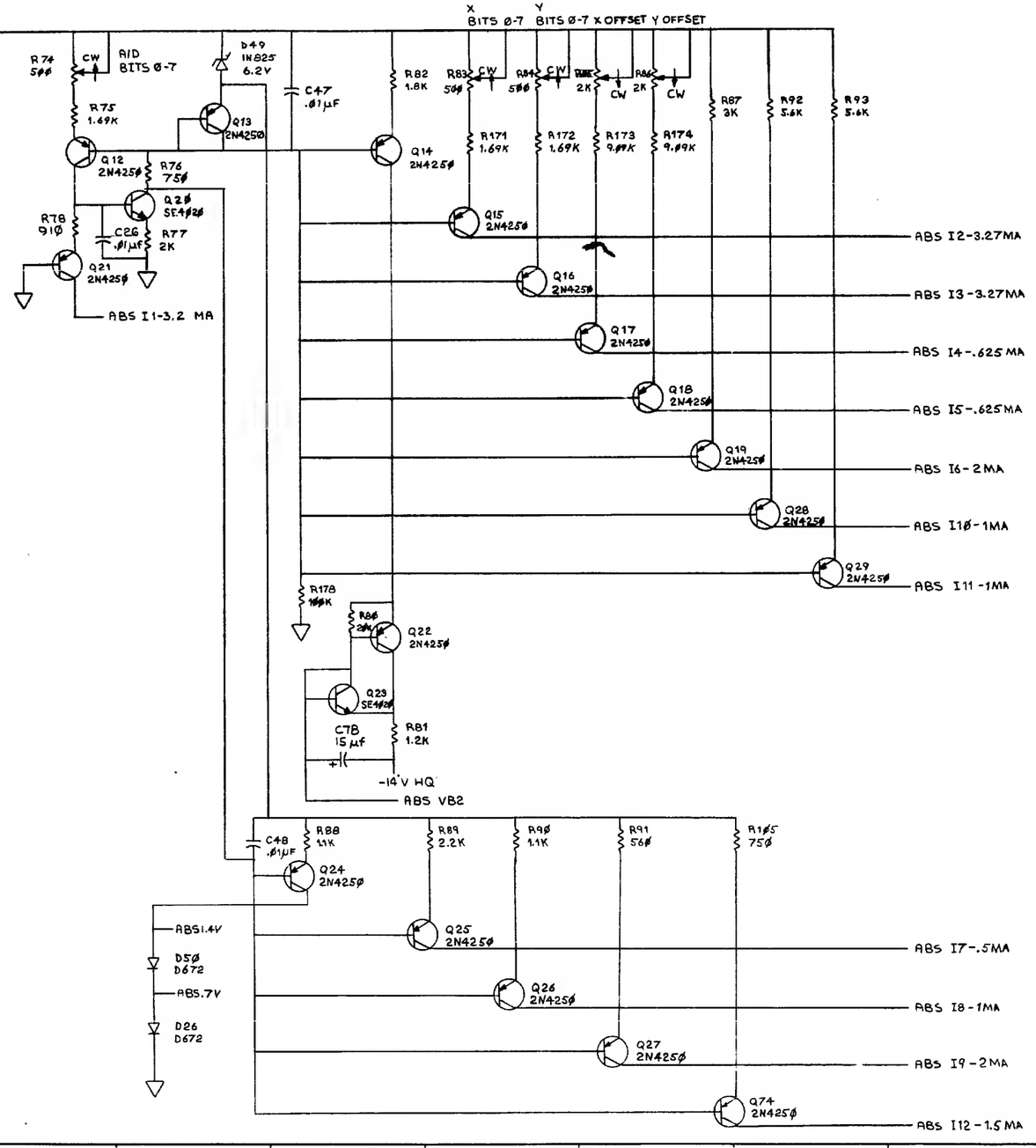
D10 D672 — D11 D672 — C16 15µF — C21 15µF — C23 .01µF — L1 100µH — +14V HQ — TP-

*C79, C80, C81 NOT ON REV B

REVISIONS		
CHK	CHANGE NO.	REV.

HQP (HQ POWER)

TITLE	SIZE	CODE	NUMBER	REV.
AR 11	D	CS	M7809-0-1	E
SCALE NONE — SHEET 8 OF 16	DIST.			



REVISIONS		
CHK	CHANGE NO.	REV.

ABS (ANALOG BIAS SOURCES)

TITLE	SIZE	CODE	NUMBER	REV.
AR-11	D	CS	M78Ø9-Ø-1	E
SCALE —//— SHEET 9 OF 16	DIST.			

M78Ø9-Ø-1 E

74174 E43 AD BUF
ADC AD Ø9 H → D5 R5(1) → ADC AD BUF Ø9 H
ADC AD Ø8 H → D4 R4(1) → ADC AD BUF Ø8 H
ADC AD Ø7 H → D3 R3(1) → ADC AD BUF Ø7 H
ADC AD Ø6 H → D2 R2(1) → ADC AD BUF Ø6 H
ADC AD Ø5 H → D1 R1(1) → ADC AD BUF Ø5 H
ADC AD Ø4 H → D0 R0(1) → ADC AD BUF Ø4 H
CLR CLK

74175 E39 AD BUF
ADC AD Ø3 H → D3 R3(1) → ADC AD BUF Ø3 H
ADC AD Ø2 H → D2 R2(1) → ADC AD BUF Ø2 H
ADC AD Ø1 H → D1 R1(1) → ADC AD BUF Ø1 H
ADC AD Ø0 H → D0 R0(1) → ADC AD BUF Ø0 H
CLR CLK

74174 E63 AD STAT
BIO OUT 13 H → D5 R5(1) → ADC UNIPOLAR H
BIO OUT 11 H → D3 R3(1) → ADC AD MUX Ø3 H
BIO OUT 10 H → D2 R2(1) → ADC AD MUX Ø2 H
BIO OUT Ø9 H → D1 R1(1) → ADC AD MUX Ø1 H
BIO OUT Ø8 H → D0 R0(1) → ADC AD MUX Ø0 H
CLR CLK

74175 E77 AD STAT
BIO OUT Ø6 H → D3 R3(1) → ADC AD INT ENA (1) H
BIO OUT Ø5 H → D2 R2(1) → ADC AD CLK ENA (1) H
BIO OUT Ø4 H → D1 R1(1) → ADC AD EXT ENA (1) H
D0 R0(1)
CLR CLK

HQP AD CLK H → 7404 E48 → 7405 E47
ADC EOCP L → 7405 E47
+5V R35 1.1K
C8 220 Pf
7404 E48 → BAS B INIT L

BAS AD STAT L, BAS OUT HIGH L → 7402 E46
BAS AD STAT L, BAS OUT LOW L → 7402 E69

+5V R40 1.1K
ADC +3V
AD DONE
ADC EOCP H
7474 E45
ADC AD DONE (1) H
ADA AD INT ENA (1) H → 7400 E56 → 7404 E48 → ADC INT A H

BAS IN L, BAS AD BUF L → 7402 E46
IV A INT DONE L → 7400 E56
7402 E46 → 7474 E45 D

+5V R36 4.7K
C9 270 Pf
J1 U
R168 47
+5V D2 D672 R37 3.3K
D3 D672
EXT AD ST L
74123 E34 EXT AD ST 500NS
ADC AD CLK ENA (1) H
RTC CLK OVR FLW H → 7451 E68
ADC AD EXT ENA (1) H
ADC EXT ST (1) L
ADC EXT ST (1) H

ADC +3V
ADC EOCP H
7474 E44
ADC HOLD (1) L
ENA AD
HQP AD CLK H
TP E
ADC ENA AD (1) L
BAS INIT H → 7402 E46
ADC CLR L

ADC EOCP L → 7404 E48
+5V R39 47K
C10 220 Pf
W1
C11 560Pf
7404 E48 BIO OUT ØØH
T4123 E34
AD START
8 µSEC-W1 OUT
11µSEC-W1 IN
ADC + 3V

ADC HOLD (1) L → 7400 E28 → ADC AD STAT ØØ (1) H

AD COMP H → 7405 E47 → ADC COMP L
+5V R38 1.1K
TP1 TPG TPØ
ALL 1'S ALL Ø'S

AM2504 E26 SAR
ADC ENA AD (1) L → E
ADC CLR L → S
ADC COMP L → D
HQP AD CLK H → C
ADC AD Ø9 H
ADC AD Ø8 H
ADC AD Ø7 H
ADC AD Ø6 H
ADC AD Ø5 H
ADC AD Ø4 H
ADC AD Ø3 H
ADC AD Ø2 H
ADC AD Ø1 H
ADC AD Ø0 H
ADC EOCP L

REVISIONS
CHK	CHANGE NO.	REV.

ADC (A/D CONTROL)

TITLE	SIZE	CODE	NUMBER	REV.
AR11	D	CS	M7809-Ø-1	E
SCALE NONE	SHEET 10 OF 16	DIST.		

DEC FORM NO. 090 138

J1

CH Ø VV R5Ø 1K
CH 1 TT R51 1K
CH 2 RR R52 1K
CH 3 NN R53 1K
CH 4 LL R54 1K
CH 5 JJ R55 1K
CH 6 FF R56 1K
CH 7 DD R57 1K

2501 E5

CH 1Ø BB R58 1K
CH 11 Z R59 1K
CH 12 X R6Ø 1K
CH 13 V R61 1K
CH 14 T RG2 1K
CH 15 R RG3 1K
CH 16 N RG4 1K
CH 17 L RG5 1K

2501 E11

ADCS -5.4V
+5V
-14 V HQ
D46 D672
R66 2K
D51 D672
ADCS -4.7V
D47 1N4732A 4.7V

-14V HQ
+14V HQ

DG 501 C E6 MUX Ø
A0 A1 A2 ØE

DG 501 C E12 MUX 1
A0 A1 A2 ØE

ADCS MUX MODE
ADCS AD MUX Ø ENA H
ADCS AD MUX 1 ENA H
ADCS MUX A2 L
ADCS MUX A1 L
ADCS MUX A0 L

+14 V HQ
RG8 20K RG9 20K R7Ø 20K

ADC AD MUX ØØ H — 7416 E18 — ADCS MUX A0 L
ADC AD MUX Ø1 H — 7416 E18 — ADCS MUX A1 L
ADC AD MUX Ø2 H — 7416 E18 — ADCS MUX A2 L

+14VHQ
R71 20K R72 20K

ADC AD MUX Ø3 H — 7400 E28 — 7416 E18 — ADCS AD MUX 1 ENA H

ADC ENAA/D (1) L — 7416 E18 — R67 20K +14V HQ
7405 E47 — 7400 E28 — R169 1.1 K +5V — 7416 E18 — ADCS AD MUX Ø ENA H

ABS +1.4V — Q10 6534 D
Q11 2N5245 D
D45 D672
R73 100 K
D15 D672
-14V HQ

REVISIONS		
CHK	CHANGE NO.	REV.

ADCS (A/D CHANNEL SELECT)

TITLE	SIZE	CODE	NUMBER	REV.
AR 11	D	CS	M78Ø9-Ø-1	E
SCALE NONE	SHEET 11 OF 16	DIST.		

ABS I8- 1MA
ABS I7-.5MA
ABS I12 - 1.5 MA
AD ZERO 2K R114 CW
7.5K R175
Q41 2N4250
Q42 2N4250
+5V
1.1K R176
Q43 2N4250
Q44 2N4250
D672 D17
D672 D16
ABS+.7V
Q45 2N4250
D672 D28
D672 D29
ABS I9- 2MA
AD COMP H
Q48 2N5245
HOLD
SAMPLE
1.1K R116
Q46 SE4020
Q47 SE4020
1.1K R117
D672 D30
C46 .01µf
5.1V IN751 D31
-14V HQ
ADC HOLD(I) L
ADCS MUX NODE
ABS I6- 2MA
33 R106
100 R107
1.1K R108
TP A
Q35 2N4250
Q36 2N4250
Q40 SE 4020
392 R109
R111 392
D672 D27
1.1K R112
1.1K R113
100 PF C27
+14V HQ
D20 MCL 1301
Q49 2N5245
Q50 SE4020
TP SH S+H OUTPUT
.001µF C28
AD ENA AD H
ADC AD0B H
8881 E17
+14V HQ
2.7K R95
2.7K R94
R170 1.1K +5V
ADC UNIPOLAR H
ADC ENA AD (I) L
ADC AD 09 H
8881 E17
8881 E17
7400 E28
AD ENA AD H
ABS 1.4V Q30 6534D
ABS 1.4V Q31 6534D
7.5K R97
Q33 2N4250
ABS VB2 Q37 SE4020
200* R99 CW AD BIT 9
R101 1.2K*
-14 V HQ
7.5K R98
Q34 2N4250
ABS VB2 Q38 SE4020
*200 R100 CW AD BIT 8
R102 1.2K*
R104 1.1K
R103 1.1K
C49 .01µf
ABS I1- 3.2 MA
DACX +5V HQ
ADC AD 00 H
ADC AD 01 H
ADC AD 02 H
ADC AD 03 H
ADC AD 04 H
ADC AD 05 H
ADC AD 06 H
ADC AD 07 H
MC1408L-8 E22
C29 27pf
-14 V HQ
ADC ENA A/D (1) L
8881 E17
D672 D19
D672 D18
+14 V HQ
1.1K R118
4.7K R177
Q32 6534D
Q60 2N5460
Q70 2N 5460
4.7K R96
D672 D48
ADCS - 4.7V
ABS VB2
Q39 SE4020
2K R79
-14 V HQ

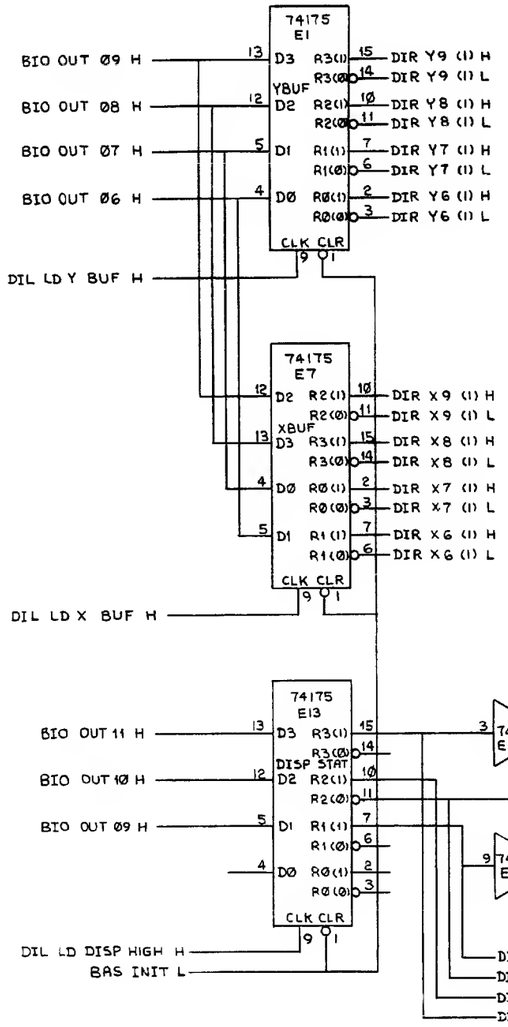
* REV B R94,95 3K
P99,100 500
R101,102 1K

REVISIONS

CHK	CHANGE NO.	REV.

AD (A/D)

TITLE	SIZE	CODE	NUMBER	REV.
AR11	D	DCS	M7809-0-1	E
SCALE NONE	SHEET 12 OF 16	DIST.		



REVISIONS		
CHK	CHANGE NO.	REV.

DIR (DISPLAY REGISTERS)

TITLE	SIZE	CODE	NUMBER	REV.
ARII	D	CS	M7809-Ø-1	E
SCALE NONE	SHEET 13 OF 16		DIST.	

M7809-Ø-1 E

+5V
J1 H
ERASE RET L
R110 15K
R119 15K
R120 10K
R121 3K
Q53 SE4020
DIL ERASE CLR H
7402 E19

W3 OUT - 20 µs
W3 IN - 80 µs
C30 .01µf
C31 3300 pf
W3
R122 20K
74123 E21

W6 OUT - 2 µs
W6 IN - 6 µs
C77 1000 pf
C32 560 pf
W6
R124 10K
74123 E21
R123 1.1K
DIL +3V

7416 E15
W4 W4A
W4 IN — INTENSIFY LOW
W4 A IN — INTENSIFY HIGH

+5V
R126 2K
R127 68
R125 3.3K
R128 1.1K
Q52 6534D
Q51 30098
DIL INTENSIFY
D32 IN746A 3.3V
D33 D672
D34 D672
W5
W5 IN — 1.4V
W5 OUT — 3.3V

J1
A DIR WRITE THRU L
B DIR DISP CH02 L
C DIL ERASE L
D DIL INTENSIFY
E DIR NONE STORE L
F DACX X OUT
H ERASE RET L
J DACY Y OUT
K
L CH 17
M
N CH 16
P
R CH 15
S
T CH 14
U EXT AD ST L
V CH 13
W
X CH 12
Y
Z CH 11
AA
BB CH 10
CC
DD CH 07
EE
FF CH 06
HH
JJ CH 05
KK
LL CH 04
MM
NN CH 03
PP -14 V HQ
RR CH 02
SS +14 V HQ
TT CH 01
UU +5 V HQ
VV CH 00
HQ GND

BAS OUT HIGH L
BAS DISP STAT L
BAS OUT LOW L
BAS X BUF L
BAS OUT LOW L
BAS Y BUF L
7402 E24
7402 E24
7402 E19
7402 E19
DIL LD DISP HIGH H
DIL LD DISP LOW H
BIO OUT 00 H
DIL LD X BUF H
DIR DISP MODE 0 (1) H
DIR DISP MODE 1 (1) H
DIL LD Y BUF H
7453 E20
7416 E15
+5V
R129 1.1K
DIL DISP ERASE (1) H
7402 E19

BAS B INIT L
DIL +3V
7474 E25
DIL DISP DONE (1) H

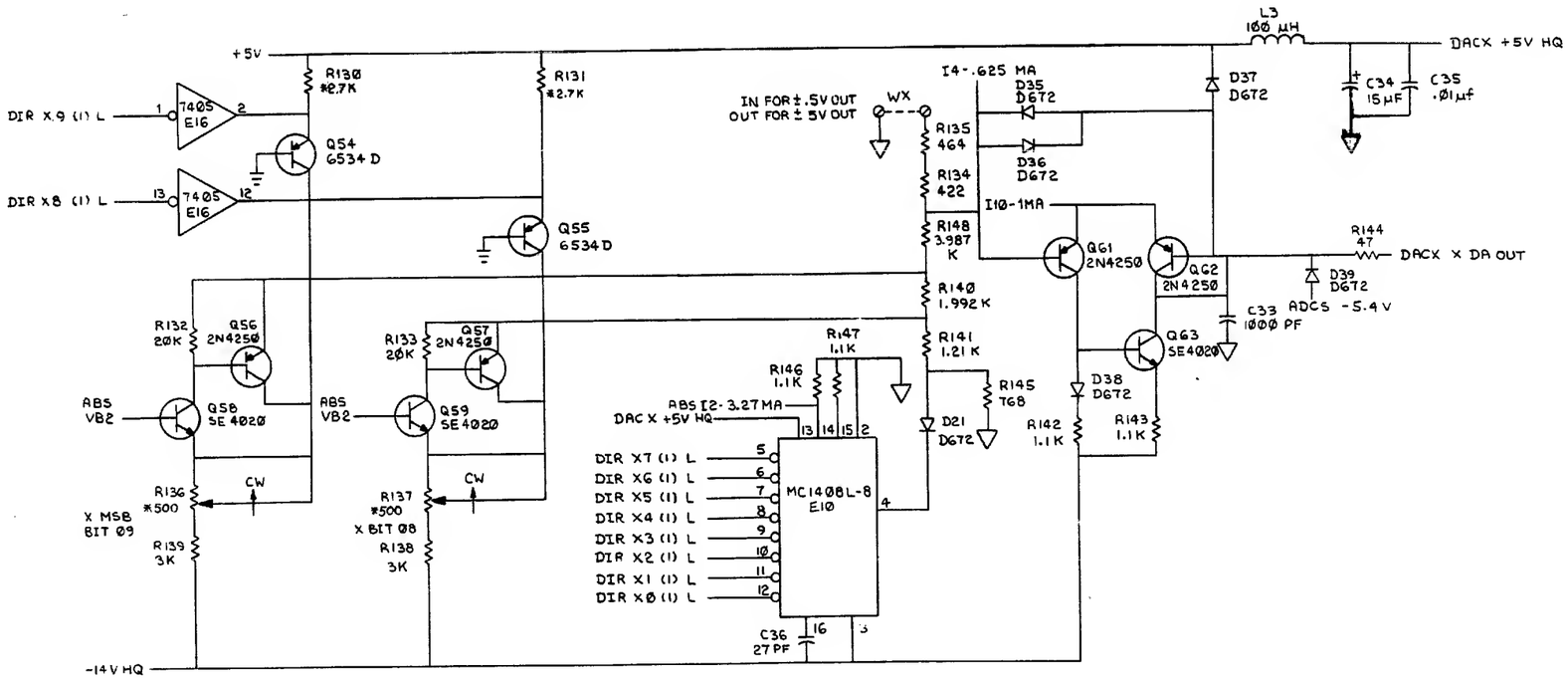
7416 E15
DIL ERASE L
DIL +3V
BIO OUT 12 H
DIL LD DISP HIGH H
7474 E23 ERASE
DIL DISP ERASE (1) H
DIR DISP INT ENA (1) H
DIL DISP DONE (1) H
7474 E25 DISP INT
DIL INT C H
DIL ERASE CLR H
BAS INIT H
IV DISP INT DONE H
7402 E24
7402 E24

REVISIONS
CHK | CHANGE NO. | REV.

DEC FORM NO. DMD 138

DIL (DISPLAY LOGIC)

TITLE AR11
SIZE CODE D CS
NUMBER M7809-0-1
REV. E
SCALE NONE
SHEET 14 OF 16
DIST.



REV B R130, R131 3K
R136, R137 1K

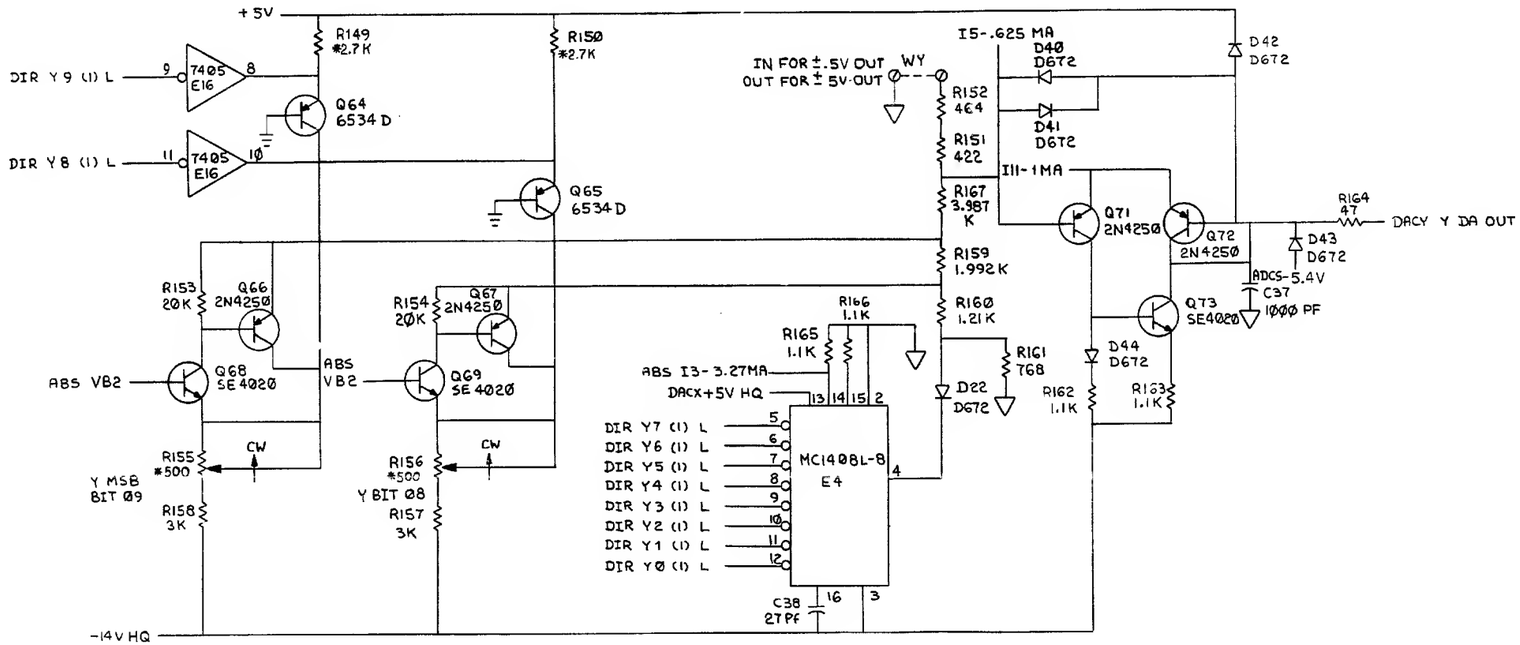
REVISIONS		
CHK	CHANGE NO.	REV.

DACX (D/A CONVERTERS)

TITLE	SIZE	CODE	NUMBER	REV.
AR11	D	CS	M7809-Ø-1	E

SCALE NONE | SHEET 15 OF 16 | DIST.

REV. E
SIZE CODE DCS NUMBER M7809-Ø-1



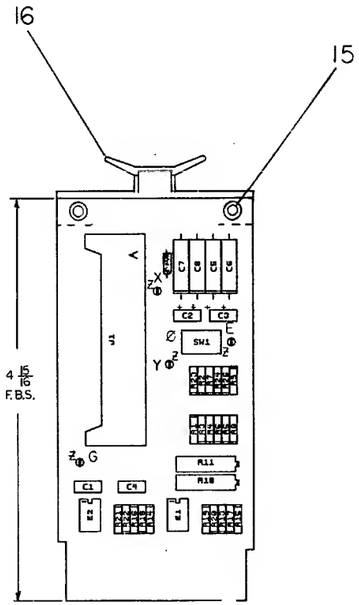
*REV B R149, R150 3K
R155, R156 1K

DACY (D/A CONVERTERS)

REVISIONS		
CHK	CHANGE NO.	REV.

TITLE	SIZE	CODE	NUMBER	REV.
AR11	D	CS	M78Ø9-Ø-1	E
SCALE NONE	SHEET 16 OF 16	DIST.		

NOTES:



REF		X-Y COORDINATE HOLE LOCATION	M-CO-G5036-0-4	1
REF		ASSY DRILLING HOLE LAYOUT	DAH-G5036-0-5	2
REF		MODULE ECO HISTORY	B-MH-G5036-0-6	3
1		ETCH CIRCUIT BOARD	5011045	4
4	C1 THRU C4	CAP. .01 µf, 100V, 20% DISC	1001610-01	5
4	C5 THRU C8	CAP. .15 µf, 20V, 10% TANT	1004812	6
1	J1	CONN. 40 PIN	1209941	7
5	R1, R13 THRU R16	RES. 100K 1/4W 1% (RN55D-1003F)	1303344	8
5	R2, R8, R23, R24, R25	RES. 4K 1/4W 1% (RN55D-4001F)	1305127	9
5	R3, R9, R17, R18, R26	RES. 1K 1/4W 1% (RN55D-1001F)	1303114	10
2	R4, R7	RES. 9.09K 1/4W 1% (RN55D-9091F)	1304855	11
6	R5, R6, R19 THRU R22	RES. 1.992K 1/4W 1% (RN55E-1992B)	1302677	12
2	R10, R11	RES. 10K POT 3/4W 10% 76 PR	1309143-10	13
2	E1, E2	IC DEC 741	1910298	14
2		EYELET	9006732	15
1		HANDLE, FLIP CHIP GREEN	9008337-01	16
1	SW1	SWITCH SPDT	1209698	17
4		SPLIT LUGS	9006735	18

QTY	REF DESIGNATION	DESCRIPTION	PART NO.	ITEM NO.

FIRST USED ON OPTION MODEL

PARTS LIST

ETCH BOARD REV B

IC TYPE	GND	+ 5V	-VCC	+VCC
DEC 741	-	-	4	7

GND AND 5V ARE USUALLY PIN 7 AND 14 RESPECTIVELY EXCEPTIONS ARE STATED ABOVE

IC PIN LOCATIONS

REV	CHANGE NO	CHK	DRN	DATE
B	G5036-00001	EC	A. FILZ	5-14-75

DEC NO	EIA NO	DEC NO.	EIA NO

SEMICONDUCTOR CONVERSION CHART

DRN.	DATE
CHK'D.	DATE
ENG.	DATE
PROJ. ENG.	DATE
PROD.	DATE
NEXT HIGHER ASSY	
SCALE NONE	
SHEET 1 OF 2	

digital EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

TITLE
WRAP AROUND

SIZE	CODE	NUMBER	REV.
D	CS	G5036-0-1	B

DIST.

DCS G5036-0-1 B

J1

CH1 TT
CHØ VV
HQGND W
CH2 RR
+5V HQ UU
CH3 NN
+14V SS
CH4 LL
-14V PP
CH17 L
ERASE RETURN H
INTENSIFY D
EXT AD ST L U
X D/A F
CH11 Z
CH13 V
ERASE C
CH14 T
WRITE THRU A
CH15 R
NON-STORE E
CH16 N
CHØ2 L B
CH1Ø BB — CH1Ø
CH5 JJ — CH5
Y D/A J
CH12 X
CH6 FF
CH7 DD
X D/A GND M
Y D/A GND K

SW1 E Ø
R1 1ØØK
R3 1K
R2 4K
+1V
R5 1.992K
R4 9.Ø9K
+2.5V
R6 1.992K
R7 9.Ø9K
-2.5V
R8 4K
R9 1K
+4V
G
X
R23 4K
R24 4K
R25 4K
R26 1K
Y
CW
R1Ø 1ØK
C1 .Ø1µf
C7 15µf
E1 741
C2 .Ø1µf
C8 15µf
CW
R11 1ØK
C3 .Ø1µf
C6 5µf
E2 741
C4 .Ø1µf
C5 15µf
R19 1.992K
R20 1.992K
CH 5
R13 1ØØK
R14 1ØØK
CH1Ø
R18 1K
R21 1.992K
R22 1.992K
R16 1ØØK
R15 1ØØK
R17 1K

D C B A

REVISIONS		
CHK	CHANGE NO	REV

TITLE	SIZE	CODE	NUMBER	REV
WRAP AROUND	D	CS	G5236-0-1	B
SCALE NONE	SHEET 2 OF 2	DIST.		

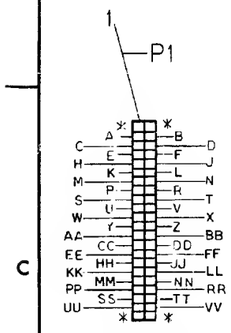
8 7 6 5 4 3 2 1

WIRE TABLE

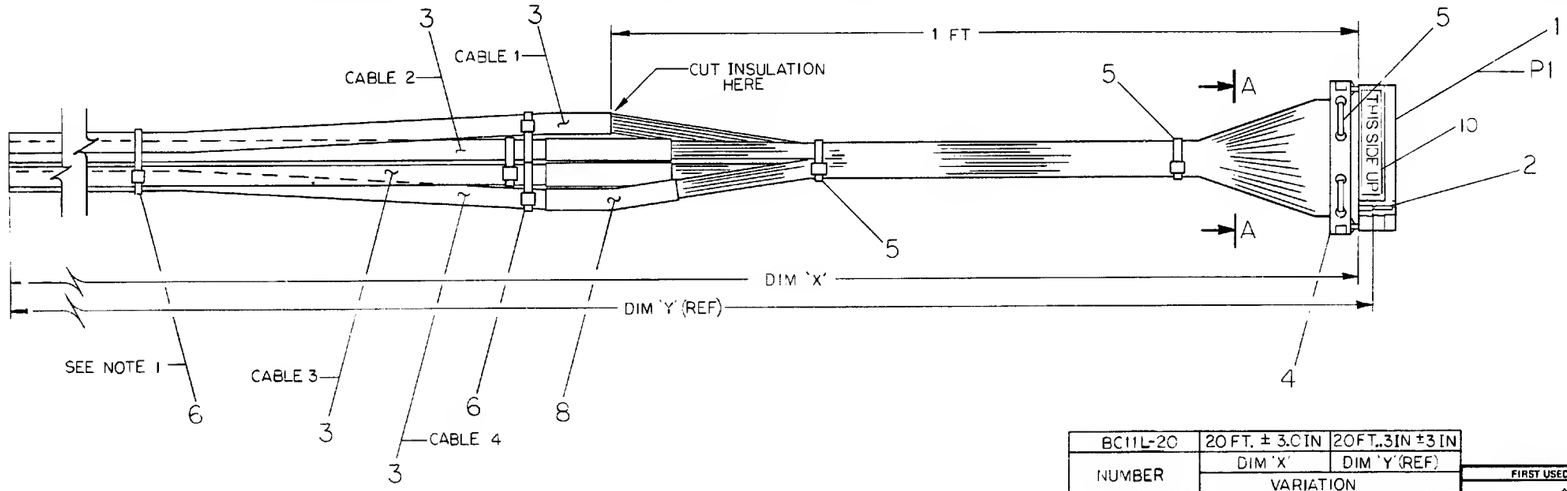
ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH	REMARKS
3	24 TWP	BLK	CABLE 1	SOLDER	P1-S	2	LOGIC GND
		BLU			P1-U	2	EXT A/D ST L
	SHIELD	—			—	—	CUT FLUSH
	24 TWP	BLK			—	—	CUT FLUSH
		YEL			P1-UU	2	+5V HQ
	SHIELD	—			—	—	CUT FLUSH
	24 TWP	GRN			P1-VV	2	A/D CH ØØ
		BLK					
	SHIELD	—			P1-MM	2,7	SEE NOTE 3
	SHIELD	—					HQ GND
	24 TWP	BLK			P1-TT	2	A/D CH Ø1
		WHT			P1-RR	2	A/D CH Ø2
	24 TWP	BRN					
		BLK		SOLDER	P1-KK	2,7	SEE NOTE 3
	SHIELD	—					HQ GND
	SHIELD	—					
	24 TWP	BLK			P1-NN	2	A/D CH Ø3
		RED			P1-LL	2	A/D CH Ø4
	24 TWP	GRN	CABLE 2				
		BLK		SOLDER	P1-HH	2,7	SEE NOTE 3
	SHIELD	—					HQ GND
	SHIELD	—					
	24 TWP	BLK			P1-JJ	2	A/D CH Ø5
		WHT			P1-FF	2	A/D CH Ø6
	24 TWP	BRN					
		BLK		SOLDER	P1-EE	2,7	SEE NOTE 3
	SHIELD	—					HQ GND
	SHIELD	—					
	24 TWP	BLK			P1-DD	2	A/D CH Ø7
		RED			P1-BB	2	A/D CH 10
	24 TWP	YEL					
		BLK		SOLDER	P1-CC	2,7	SEE NOTE 3
	SHIELD	—					HQ GND
	SHIELD	—					
	24 TWP	BLK			P1-Z	2	A/D CH 11
3		BLU					

WIRE TABLE (CON'T.)

ITEM NO.	DESCRIPTION AWG	DESCRIPTION COLOR	FROM CONNECTION	FROM WITH	TO CONNECTION	TO WITH	REMARKS
3	24 TWP	GRN	CABLE 3		P1-X	2	A/D CH 12
		BLK		SOLDER	P1-AA	2,7	SEE NOTE 3
	SHIELD	—					HQ GND
	SHIELD	—					
	24 TWP	BLK			P1-V	2	A/D CH 13
		WHT			P1-T	2	A/D CH 14
	24 TWP	BRN					
		BLK		SOLDER	P1-Y	2,7	SEE NOTE 3
	SHIELD	—					HQ GND
	SHIELD	—					
	24 TWP	BLK			P1-R	2	A/D CH 15
		RED			P1-N	2	A/D CH 16
	24 TWP	YEL					
		BLK		SOLDER	P1-W	2,7	SEE NOTE 3
	SHIELD	—					HQ GND
	SHIELD	—					
	24 TWP	BLK			P1-L	2	A/D CH 17
		BLU			P1-A	2	WRITE THRU
	24 TWP	GRN	CABLE 4		P1-B	2	DISP CLK/ENB L2
		BLK			—	—	CUT FLUSH
	SHIELD	—			P1-C	2	ERASE
	24 TWP	WHT			P1-D	2	INTENSIFY
		BLK			—	—	CUT FLUSH
	SHIELD	—			P1-E	2	NON STORE
	24 TWP	BRN			P1-H	2	ERASE REF
		BLK			—	—	CUT FLUSH
	SHIELD	—			P1-P	2	LOGIC GND
	24 TWP	RED			—	—	CUT FLUSH
		BLK			—	—	CUT FLUSH
	SHIELD	—			P1-F	2	X OUT
	24 TWP	YEL					
		BLK		SOLDER	P1-M	2,7	SEE NOTE 3
	SHIELD	—					HQ GND
	SHIELD	—		SOLDER	P1-K	2,7	SEE NOTE 3
	24 TWP	BLK					HQ GND
3		BLU			P1-J	2	Y OUT



VIEW A-A
SCALE: NONE
* NOT USED



BC11L-20	20 FT. ± 3.0 IN	20 FT. 3 IN ± 3 IN
NUMBER	DIM 'X'	DIM 'Y' (REF)
	VARIATION	
	LEGEND	

NOTES:
1. PLACE CABLE TIES APPROXIMATELY EVERY 10 IN. AND WHEREVER INDICATED.
2. USE ITEM #9 (CABLE MARKERS) TO IDENTIFY CABLES BY NUMBER. POSITION APPROXIMATELY 2 FT. FROM EACH END.
3. BLACK WIRE (FROM #24 TWP) AND SHIELD TO BE CUT APPROXIMATELY .7" FROM CABLE INSULATION. BLACK WIRE (STRIPPED) AND SHIELD TO BE TWISTED AND SOLDERED TO BLACK IPVC (ITEM #7, APPROXIMATELY 12" LG.)

QTY.	DESCRIPTION	PART NO.	ITEM NO.
	LABEL, THIS SIDE UP		10
A/R	CABLE MARKERS		9
A/R	TUBING, SHRINK BLK	9107685	8
A/R	WIRE, #22 AWG IPVC BLK	9107350-00	7
A/R	CABLE TIE	9007880	6
A/R	CABLE TIE	9007031	5
1	STRAIN RELIEF	12111166	4
A/R	CABLE, BELDEN 8778	1700010	3
38	PIN, BERG (47704)	12109949-6	2
1	CONN. HOUSING, 40 PIN	12109918-15	1

PARTS LIST

FIRST USED ON OPTION/MODEL: A7..

DIMENSIONAL TOLERANCE
DIMENSIONS ARE MILLIMETERS / INCHES
UNLESS OTHERWISE SPECIFIED
MILLIMETERS: X.XX = ±0.10, X.X = ±0.5, X = ±1
INCHES: .XXX = ±.005, .XX = ±.02, X = ±.1
ANGLES: 45° 30'
THIRD ANGLE PROJECTION
REMOVE BURRS AND BREAK SHARP CORNERS SURFACE QUALITY ✓
MATERIAL: SEE PARTS - ST
FINISH: —

		DATE
DRN.	Carl Mc'Ly	6-19-74
CHK'D.		DATE
ENG.		DATE 6-25-74
PROJ. ENG.		DATE 6-21-74
PROD.		DATE 6-21-74

NEXT HIGHER ASSY. —

digital

TITLE: CABLE, BC11L

SIZE: D | CODE: UA | NUMBER: BC11L-0-0 | REV: A
SCALE: 1/1
SHEET 1 OF 1
DIST.

REVISIONS			
CHK	CHANGE NO.	REV.	
	BC11L V0001	A	A.C.FILZ

DEC FORM NO. DRD 100-9

BC11L-0-0 REV A

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 9/26/74

TITLE AR11 System Installation/Acceptance Procedure

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

TABLE OF CONTENTS

ENG	APPD	SIZE	CODE	NUMBER	REV
[illegible] 9/30/74	[illegible]	A	SP	AR11-Ø-4	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 107

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AR11 System Installation/Acceptance Procedure

1.0 SCOPE

This procedure covers the installation and acceptance of an AR11 in a PDP11 system. It is anticipated that the procedure will be used in one of the following situations:

1.1 Installation and acceptance of sn AR11 on a PDP11 system in an in-house FA & T system integration area.

1.2 Add-on installation and acceptanc of an AR11 on an existing PDP11 system in the field.

1.3 Acceptance of an AR11 on a new PDP11 system upon installation at a customer site.

1.4 On-going AR11 verification testing at intervals over the life of a given system.

2.0 AR11 MOUNTING/CONFIGURATION CONSIDERATIONS

2.1 The AR11 is a one-module option which interfaces with a PDP11 through a hex SPC slot. A hsx SPC slot is one of the following:

2.1.1 One of the two middle slots of a DD11-B, C or E four-slot prewired system unit.

2.1.2 One of the seven middle slots of a DD11-D or F nine-slot prewired double system unit.

2.1.3 Any processor-mounted SPC slot with physical room for a hex module.

SIZE	CODE	NUMBER	REV
A	SP	AR11-Ø-4	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 2 OF 19

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AR11 System Instalation/Acceptance Procedure

2.2 The AR11 may be mounted in any hex SPC slot and will opsrate within specification with no configuration restrictions whatsoever regarding physical proximity to processor, memory, or other options. AR11 analog performance may be further optimized beyond specifics-tion levels by mou:ting in an electricslly quiet environment. Consequently, if a choice is available in configuring s system, the AR11 should be mounted away from the processor and memory modules.

2.3 Cabling

The AR11 is interfaced to the outside world by means of either a BC08-R flat cable to an H322 distribution panel, a BC11-L Berg-to-open end cable, or a user-built cable. In either of the latter two cases, in a 10½" or 5¼" mounting box. the next slot (on the component side of the AR11) should not contain another hex SPC module, in order to leave room for the AR11 cable to double back and exit past the top of the module.

2.4 Bus Addresses

The AR11 starting address may be set at any address between 760ØØØ and 77776Ø (in increments of 2Ø) by means of a jumper and switches on the module. The preferred starting address is 77Ø4ØØ. Use of any other starting address will necessitate patches to the AR11 diagnostics, as well as to system software (such as RT-11 lab applications and SPARTA) which supports the AR11. The AR11 diagnostics (Test I - logic and Test III - wraparound) support multiple

SIZE	CODE	NUMBER	REV
A	SP	AR11-Ø-4	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 3 OF 19

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AR11 System Installation/Acceptance Procedurs

AR11's automatically, provided that ths AR11's occupy a sequential block of addresses 2Ø apart, and provided thst the address following the last AR11 is unused. For example, in a system with a single AR11 at 77Ø4ØØ, the address 77Ø42Ø should not be used; a system with three AR11's should have the AR11's at 77Ø4ØØ, 77Ø42Ø and 77Ø44Ø, with the address 77Ø46Ø unused. If, in configuring a system, it is necessary to use the address which is 2Ø higher than the last AR11 address, patches will be necessary to diagnostics Test I and Test III, and these disgnostics will then test only one AR11 at a time. (See section 4 for patches)

2.5 Vectors

The AR11 vector space may start in increments of 2Ø up to a maximum of 76Ø by means of switches on the module. The preferred vector is 34Ø. Use of any other vector will necessitate patches to the AR11 diagnostics, as well as to system software which supports the AR11. For AR11 diagnostics Test I and Test III to work properly with multiple AR11's in a system, ths AR11 vectors should be in sequential order, 2Ø apart. For example, in a system with three AR11's at 77Ø4ØØ, 77Ø42Ø, and 77Ø44Ø, the vectors should be 34Ø, 36Ø and 4ØØ respectively.

3.0 AR11 INSTALLATION

3.1 Based on the above considerations, choose a hex SPC mounting slot, starting address, and vector for the AR11 to be installed.

SIZE	CODE	NUMBER	REV
A	SP	AR11-Ø-4	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 4 OF 19

3.2 Set up the starting address in the following manner:

3.2.1 For addresses between 77ØØØØ and 77776Ø, leave W4 connected. For addresses between 76ØØØØ and 76776Ø, disconnect W4 and connect W4A.

3.2.2 Set up address switches (S1) per figure 1 and figure 2. Switches are set "on" for a Ø and "off" for a 1.

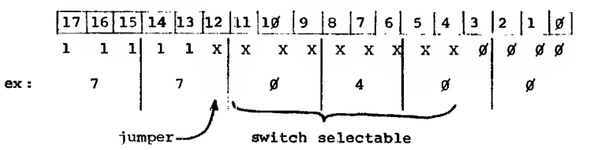


Figure 1: AR11 Address Selection

3.3.3 Example

To set up starting address 77Ø4ØØ, leave W4 connected, set all S1 switches "on" except for the bit 8 switch.

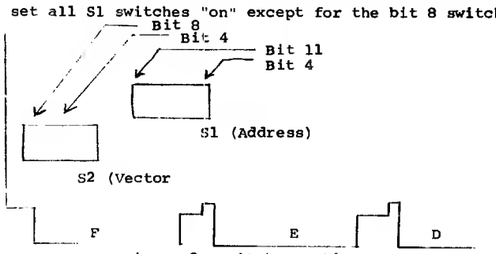


Figure 2: Switch Locations

3.3 Set up the vector in the following manner:

3.3.1 Set up vector switches (S2) per figure 2 and figure 3. Switches are set "on" for a 1 and "off" for a Ø. (Note that this is opposite to the address switches.)

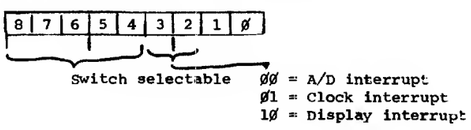


Figure 3: AR11 Vector Selection

3.3.2 Example

To set up a vector of 34Ø, the bit 7, 6, and 5 switches are "on" and the bit 8 and 4 switches are "off".

3.4 Re-install the covers on switch-packs S1 and S2.

3.5 Install the module in the selected hex SPC slot.

3.6 If the system contains an H322 signal distribution panel, connect the AR11 and H322 by means of a BCØ8-R Berg-to-Berg cable. If the system includes a BC11-L Berg-to-Berg end cable, do not install the cable at this time. Instead, install the BCØ8-R cable which is to be used with the G5036 wraparound module for acceptance testing. The BC11-L is to be installed upon completion of acceptance testing.

3.7 Install the 17-00021 electromagnetic shields on both sides of the AR11.

3.8 Conduct an acceptance test per section 4 below.

4.0 AR11 ACCEPTANCE

4.1 Test Flow

AR11 acceptance testing flow is shown in figure 4.

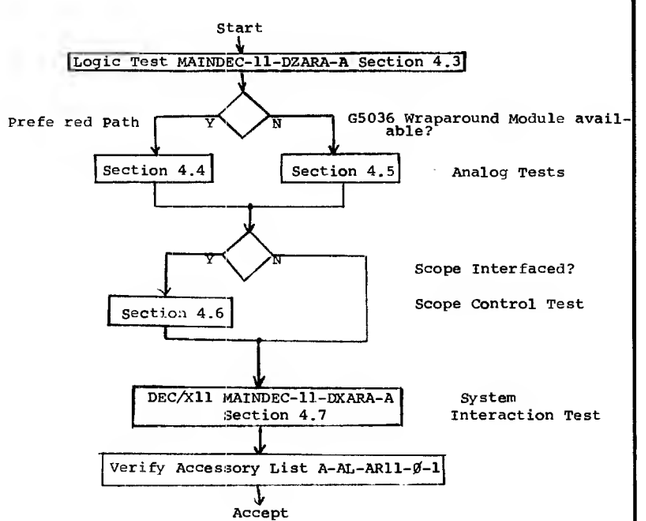


Figure 4: AR11 Acceptance Flow

In every case, AR11 acceptance begins with a complete test of the AR11 logic, described in section 4.3 below.

If a G5036 wraparound module is available, the preferred path is taken for analog testing, described in section 4.4 below. This is the normal path taken for in-house acceptance, field installation acceptance, and on-going AR11 analog verification testing by field service personnel and by users who have purchased the BG5036 maintenance kit. The analog testing path described in section 4.5 below is for on-going AR11 analog verification testing by users who have not purchased the BG5036 maintenance kit.

The scope control test, described in section 4.6, is to be run on those systems in which the AR11 is interfaced to an XY display scope or storage scope.

The DEC/X11 system interaction test, described in section 4.7, is to be run on all systems with AR11. The AR11 DEC/X11 module tests for the presence of the wraparound module and chooses one of two routines accordingly. If the G5036 wraparound module is available, it should be connected to the AR11 during DEC/X11 testing. However, DEC/X11 can be run without the wraparound module without sacrificing validity, by users who have not purchased the BG5036 maintenance kit.

4.2 Equipment and Diagnostics Required

4.2.1 PDP11 system. with AR11 and console device.

4.2.2 Calibrated DC Voltage Source EDC model MV116 or equivalent.

4.2.3 BG5036 maintenance kit: *

4.2.3.1 G5036 wraparound module

4.2.3.2 BC08-R Berg-to-Berg cable

4.2.4 MAINDEC-11-DZARA-A AR11 Test I (logic)

4.2.5 MAINDEC-11-DZARB-A AR11 Test II (analog)

4.2.6 MAINDEC-11-DZARC-A AR11 Test III (wraparound)*

4.2.7 MAINDEC-11-DXARA-A AR11 DEC/X11 module

*Not required for user's on-going verification testing

4.3 Logic Test

Load and run the logic test diagnostic MAINDEC-11-DZARA-A. Under the following conditions, no patches are required: First (or only) AR11 at address 77Ø4ØØ, vector at 34Ø; additional AR11 addresses and vectors 2Ø apart and sequential, e.g. 77Ø42Ø and 36Ø, 77Ø44Ø and 4ØØ, etc; address 2Ø higher than last AR11 address unused, e.g. 77Ø42Ø in system with one AR11, 77Ø46Ø in system with three AR11's. Otherwise, patch:

a) 136Ø/ AR11 starting address (first AR11)

b) 1362/ AR11 vector (first AR11)

c) 1526/ 5ØØ3 ; inhibit testing more than one AR11.

Without patch (c), the diagnostic automatically tests all the AR11's installed in the system (with sequential addresses 2Ø

apart) in each pass. The diagnostic must complete at least three passes without error with iterations or ten passes without error without iterations (SW11 = 1).

4.4 Analog Tests (using G5036 wraparound module)

4.4.1 For each AR11 in the system connect the AR11 to a G5036 wraparound module by means of a BC08-R Berg-to-Berg cable. For AR11's which are interfaced to H322 signal distribution panels, the BC08-R cable which normally connects to the H322 should be disconnected from the H322 and connected to the G5036. For AR11's without an H322, the BC08-R cable should come out of the processor box and cabinet. Maximum BC08-R cable length should be 12 feet. *Important Note: The BC08-R cable should be connected "upside-down" at the G5036 end, i.e. A to VV rather than A to A.

4.4.2 Set the switch on the G5036 module to the "E" position. Connect the EDC voltage source signal output to the "E" split lug on the G5036. Connect the EDC voltage source return to the "G" split lug on the G5036. The EDC should be floating to avoid ground loops. The EDC leads should be short and shielded if possible. The EDC output is now connected to the AR11 A/D channel Ø input.

4.4.3 Load the analog test diagnostic MAINDEC-11-DZARB-A. This diagnostic only tests one AR11 at a time. For an AR11 at address 77Ø4ØØ and vector 34Ø, no patches are needed.

Otherwise, patch:

a) 12Ø4/ AR11 starting address

b) 12Ø6/ AR11 vector

Start the program at location 2ØØ, select Test C (calibration test), and when requested, type 'I' for internal A/D starts. Set SW1Ø = 1 to force console printout of the converted value. Select channel Ø bipolar by leaving all other front console switches at Ø.

Set up the EDC for the input voltage indicated in column A and monitor the conversion result. It should be the value in column B, with a ±1 tolerance.

A	B
-1.875 Volts	Ø2ØØ ±1
0	1ØØØ ±1
+1.875 Volts	16ØØ ±1

4.4.4 Set the switch on the G5036 module back to the "Ø" position. The AR11 A/D channel Ø input now sees a ground, the desired input for wraparound testing. The EDC may now be disconnected.

4.4.5 Load and run the wraparound diagnostic MAINDEC-11-DZARC-A. No patches are required if the following conditions are met: First (or only) AR11 at address 77Ø4ØØ, vector at 34Ø; additional AR11 addresses and vectors 2Ø apart and sequential, e.g. 77Ø42Ø and 36Ø, 77Ø44Ø and 4ØØ, etc.; address 2Ø higher than

last AR11 address unused, e.g. 77Ø42Ø in systems with one AR11, 77Ø46Ø in system with three AR11's. Otherwise, patch:

a) 1334 / AR11 starting address (first AR11)

b) 1336 / AR11 vector (first AR11)

c) 145Ø / 5ØØ3 ; inhibit testing more than one AR11.

Without patch (c), the diagnostic automatically tests all the AR11's installed in the system (with sequential addresses 2Ø apart) in each pass. The diagnostic must complete at least two passes without error.

The wraparound diagnostic tests the following:

a) Scope intensify pulse, A/D external start

b) Storage scope hand-shaking logic-erase return, etc.

c) Scope control output logic high and low levels

d) Analog power supply levels

e) Functional check on all 16 channels of A/D input

f) A/D input bias current

g) Calibration of XD/A vs. A/D, YD/A vs. A/D

h) Linearity of XD/A vs. A/D, YD/A vs. A/D

i) Differential Linearity of A/D, XD/A, YD/A

j) A/D inter-channel settling, plus full-scale and minus full-scale

k) Noise levels - rms and peak - A/D bipolar, A/D unipolar, XD/A, YD/A

1) Offset - A/D bipolar, A/D unipolar, XD/A, YD/A

Numerical results of the above tests can be printed out, for the edification of the test operator, by setting front console SW12 = 1.

4.5 Non-wraparound Analog Tests

This section may be performed in lieu of section 4.4 for ongoing AR11 analog verification testing by users who have not purchased the BG5036 maintenance kit.

4.5.1 Load the analog test diagnostic MAINDEC-11-DZARB-A. This diagnostic tests only one AR11 at a time. For an AR11 at address 77Ø4ØØ and vector 34Ø, no patches are needed. Otherwise, patch:

a) 12Ø4 / AR11 starting address

b) 12Ø6 / AR11 vector

4.5.2 A/D Calibration and Linearity

Start the program at location 2ØØ, select Test C (calibration test), and when requested, type 'I' for internal A/D starts. If the AR11 is interfaced to a scope, the results will appear on the screen. If the AR11 is not interfaced to a scope, set front console SW1Ø = 1 to force console printout of the converted values.

Connect the EDC output to the input of the A/D channel

to be tested. Connect the EDC return to one of the A/D input grounds. The EDC should be floating to avoid ground loops. The EDC leads should be short and shielded if possible. Select the desired A/D input channel using front console SWØ3:SWØØ.

Set up the EDC for each input voltage indicated in column A and monitor the conversion result. It should be the value in column B, with a ±1 tolerance.

A	B	C
-2.500 Volts	ØØØØ ±1	0
-1.875 Volts	Ø2ØØ ±1	+.625 Volts
-1.250 Volts	Ø4ØØ ±1	+1.250 Volts
-.625 Volts	Ø6ØØ ±1	+1.875 Volts
0	1ØØØ ±1	+2.500 Volts
+.625 Volts	12ØØ ±1	+3.125 Volts
+1.250 Volts	14ØØ ±1	+3.750 Volts
+1.875 Volts	16ØØ ±1	+4.375 Volts

Set front console SWØ5 = 1, for unipolar input range. Set up the EDC for each input voltage indicated in column C and monitor the conversion result. It should be the value in column B, with a ±1 tolerance.

4.5.3 A/D Noise

The AR11 A/D's noise level can be measured in one of two manners. Each involves a burst of 512 conversions. If the average of the 512 conversions is centered within a nominal-width (1 LSB) state, the "tails" of the noise distribution can be observed in the (average +1) and (average -1) states. For

rms noise levels less than the ½ LSB spec, at least 490 conversions are in the center (average) state.

4.5.3.1 The first method of noise measurement can only be done when the AR11 is interfaced to an oscilloscope. Using this method, it is easy to center the EDC voltage within a single state, but it is necessary to count the number of conversions in the (average +1) and (average -1) states.

Select Test C (calibration test), and when requested, type 'I' for internal A/D starts. Select the desired A/D input channel using front console SWØ3:ØØ. Connect the EDC output to the input of the channel being tested as in section 4.5.2 above. A burst of 512 conversion is displayed across the screen, with four ±8 LSB "markers" superimposed on the trace. Adjust the EDC voltage so that the trace is exactly centered within a state (equal number of plus and minus "glitches"). At this input voltage, set SWØ6 = 1, to discontinue sampling and freeze the last 512-point burst on the screen. Count the number of conversions in the (average +1) and (average -1) states. This number should be less than 22_{10}, i.e. there must be at least 490 conversions in the center state.

4.5.3.2 The second method of noise measurement does not

require the AR11 to be interfaced to a scope.

Select Test D (repeatability test), and when requested, select the desired channel, and select a count spread of Ø, to force printouts of all distributions. Connect the EDC to the desired channel as in section 4.5.2 above. Observe the distributions printed out, and adjust the EDC voltage such that the distribution is centered in the "Av" state, with equal numbers of conversions in the "+1" and "-1" columns. The number in the "Av" column must be 490 or greater.

4.5.4 Inter-channel Settling

Inter-channel settling is tested by connecting two voltages which are at opposite ends of the A/D input range to two different channels. For example, connect -2.4 Volts to the channel Ø input and +2.4 Volts to the channel 1 input and run with bipolar input range (±2.5 Volts) by selecting channels Ø and 1, or connect +.1 Volts to the channel Ø input and +4.9 Volts to the channel 1 input and run with unipolar input range (0 to +5 Volts) by selecting channels 4Ø and 41. In the following description, it is assumed that -2.4 Volts and +2.4 Volts are connected to channels Ø and 1.

Select Test E (recovery test), and when requested, type "Ø, 1" for the positive settling test and "1, Ø" for the negative settling test. A series of eight conversion values is

then typed out. In each case, the first value typed out should be within one count of the average of the remaining seven values. (If the remaining seven values are on the borderline between two states, change the input voltage by 2.5 mV and repeat the test.)

4.6 Scope Control Test

This test is done only if the AR11 is interfaced to an oscilloscope. The analog test diagnostic MAINDEC-11-DZARB-A must be loaded (and patched for proper address and vector if necessary) per section 4.5.1 above. Select Test B (display).

The program will loop through the following eight "pictures": horizontal line, vertical line, square, X, settling test square wave, character set, channel 1 - channel 2, descending horizontal line. Observe these pictures for linearity, dot spacing, and lack of noise or jitter.

Set SWØ8 = 1 to select a fixed "picture". Set SWØ2 = 1 to select the settling test square wave. With SWØ7 = Ø observe settling in the horizontal direction; with SWØ7 = 1 observe settling in the vertical direction. Maximum settling error should be "1 dot".

If the scope which is interfaced to the AR11 is a VR14, with SWØ8 = 1, set SWØ2:ØØ = 6. With the VR14 switched to "both", "Channel 1" and "Channel 2" should appear on the screen. With the

VR14 switched to "channel 1", "Channel 1" should appear on the screen; likewise for "channel 2".

4.7 DEC/X11 System Integration Test

The system exerciser is configured using the AR11 exerciser module MAINDEC-11-DXARA-A along with modules for all other options present. The G5036 wraparound module should be installed per section 4.4.1 above. The AR11 exerciser measures (and compares to spec limits) rms and peak noise levels on A/D, X D/A, and Y D/A. All A/D conversions are started on clock overflow after a random number has been loaded into the clock buffer register. Since the system is being exercised in the background at the time the A/D conversions start, the noise levels measured are true worst case levels, under conditions of full system interaction.

For purposes of on-going verification testing by a user who has not purchased the BG5036 maintenance kit, the DEC/X11 module may be run without wraparound. Under this condition, the program senses the absence of the G5036 wraparound module and goes to a routine which takes conversionson each of the 16 channels and displays them on the screen of the scope driven by the AR11. Each channel is displayed in turn for about three seconds.

5.0 AFTER ACCEPTANCE

5.1 Remove the G5036 wraparound module. It is not shipped with the AR11.

5.2 If the system includes an H322 signal distribution panel, reconnect the BC08-R cable to the H322. If the system does not include an H322, remove the BC08-R cable. It is not shipped.

5.3 If the system includes a BC11-L cable, it should be installed at this time. If the AR11 is in a new version 10½" or 5¼" mounting box, so that the BC11-L cable cannot go straight out the back, the BC11-L cable must double back and exit past the top of the module.

5.4 Verify that all items on the AR11 accessory list A-AL-AR11-Ø-1 are present and properly packed for shipment.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 9/16/74

TITLE AR11 Circuit Description

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

ENG	APPD	SIZE	CODE	NUMBER	REV
[signature] 9/19/74	[signature]	A	SP	AR11-Ø-5	

DEC FORM NO DEC 16-(392)-1070-N971
DRA 107

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AR11 Circuit Description

1.0 INTRODUCTION

1.1 The AR11 is a one-module real-time analog subsystem that interfaces with the PDP-11 family of computers via a hex SPC slot. Included on the AR11 module are the following:

1.1.1 Bus Control, with switch-selectable address.

1.1.2 Interrupt Control, with switch-selectable vector.

1.1.3 A/D Converter, with 16-channel multiplexer and sample-and-hold.

1.1.4 Real-time Clock, with five crystal-based frequencies, external input, and an 8-bit counter.

1.1.5 Display Control, with two 10-bit D/A converters.

1.1.6 Analog Power Supply.

1.2 The following material should be referenced when using this document:

1.2.1 M78Ø9 (AR11) circuit schematics D-CS-M78Ø9-Ø-1.

1.2.2 AR11 User's Guide DEC-11-HARUG-A-D

1.2.3 PDP11 Processor Handbook

1.2.4 Manufacturer's manual for XY display scope or storage scope being used with the AR11.

1.3 Reading M78Ø9 Prints

At the bottom right corner of each M78Ø9 circuit schematic page is the page title, e.g. BAS (BUS ADDRESS SELECT). The symbol preceding the parentheses is the page mnemonic. Each

SIZE	CODE	NUMBER	REV
A	SP	AR11-Ø-5	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AR11 Circuit Description

signal generated on a given page has that page's mnemonic in front of it for page cross-reference purposes. For example, BAS ENABLE L originates on the BUS ADDRESS SELECT page, and is low when ENABLE is asserted.

2.0 BUS CONTROL

The AR11 Bus Control consists of BAS (BUS ADDRESS SELECT), BIO (BUS IN/OUT) and DM (DATA IN MULTIPLEXERS), pages 3, 4 and 5 of the M78Ø9 schematics.

2.1 Bus Address Select

The purpose of the bus address select logic is to recognize one of the eight AR11 register addresses on the Unibus address lines, select the register for input or output data transfer upon receipt of MSYN L from the processor, and to acknowledge receipt of MSYN L by sending SSYN L back to the processor.

Bus address lines A17 L through AØ4 L are used to recognize that one of eight AR11 registers is being addressed. Bus address lines AØ3 L through AØ1 L are decoded to determine which of these eight registers is being addressed. BUS AØØ L is used to determine high or low byte within the word, in conjunction with BUS CØØ L, which is low for a computer output byte operation and high for an output word operation.

BUS A11 L through AØ4 L are compared with the state of the address select switches using "exclusive or" circuits E87 and E94.

SIZE	CODE	NUMBER	REV
A	SP	AR11-Ø-5	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AR11 Circuit Description

The "exclusive or" output is high when A11 through AØ4 match the switch address. When this occurs, and the E62-3 output is high, the AR11 has recognized its address, and BAS ENABLE L is asserted. The E62-3 output is high with BUS MSYN L asserted and 77XXXX (W2 connected) or 76XXXX (W2A connected) on the bus address lines. Thus, as a function of the address switches, the AR11 can have any address from 76ØØØØ through 76776Ø with W2A connected and from 77ØØØØ through 77776Ø with W2 connected.

AR11 address selection is further illustrated in figure 1:

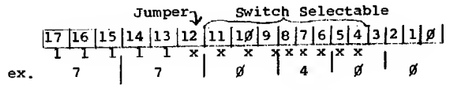


Figure 1: AR11 Address Selection

Location of the address switches on the module is shown in figure 2. The switches are set "on" for a Ø and "off" for a 1, i.e. to set up 77Ø4ØØ, all switches are "on" except for the bit 8 switch.

SIZE	CODE	NUMBER	REV
A	SP	AR11-Ø-5	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

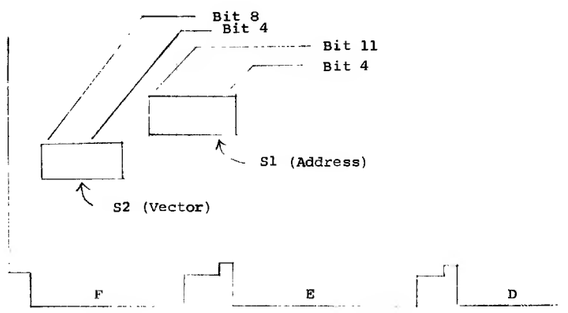


Figure 2: Switch Location

When BAS ENABLE L is asserted, the address decoder E74 is enabled. As a function of address lines BAS AØ3H through BAS AØ1H, E74 selects one of the eight AR11 registers and asserts the corresponding select line, per Table 1.

After a delay of approximately 75 nsec, determined by the (R1 + R2) C1 time constant, BAS ENABLE L causes the slave synch line SSYN L to be asserted, informing the processor that the selected data has been received or is present on the data lines.

BUS INIT L is buffered to produce BAS INIT L, BAS B INIT L, and BAS INIT H, which clear all the registers and flags, with the exception of the scope control ready flag. Ths INIT signal occurs

on start key depression, power up, or RESET instruction.

TABLE 1: REGISTER ADDRESSES

AØ3 H	AØ2 H	AØ1 H	Addrsss Selected
L	L	L	A/D Status
L	L	H	A/D Buffer
L	H	L	Clock Status
L	H	H	Clock Preset Buffer
H	L	L	Display Status
H	L	H	X Buffer
H	H	L	Y Buffer
H	H	H	Clock Counter

2.2 Bus In/Out

The Unibus has bidirectional data paths, which are interfaced to the AR11 using 8641 (8838) recsiver/transmitter chips. The outputs of the data multiplexers (DM BIT ØØ H, DM BIT Ø1 H, etc.) are impressed on the Unibus data lines (BUS DØØ L, BUS DØ1 L, etc.) for computer input operations. This occurs when BAS IN L and BAS ENABLE L are asserted, signifying an input operation when the AR11 has recognized its address.

The data lines enter the AR11 from the Unibus through the inverters, and become the BIO OUT XX H signals.

2.3 Data In Multiplsxers

The DATA IN MULTIPLEXERS use 74151 and 74157 multiplexer chips to sort out the data from the eight different registers. The selected register outputs become the DM BIT XX H signals, which are passed on to the Unibus by the BUS IN/OUT logic.

AØ3 H, AØ2 H and AØ1 H are used as address inputs by the 74151 one-of-eight multiplexers, to select the desired register, for bits Ø through 9. Bits 1Ø through 13 are only contained in the A/D Status Register and Display Status Register. Therefore, they are able to use a 74157 quad one-of-two multiplexer chip. When AØ2 H and AØ1 H are low, E55-15 is low, enabling the 74157. When this occurs, either the A/D or Display Status register is being selected. BAS AD STAT L goes to pin 1 of the 74157, to select which of the two registers is active.

3.0 INTERRUPT CONTROL

The interrupt control handles three distinct interrupts. These may come from the A/D (INT A H), the Realtime clock (INT B H) or the scope control (INT C H). The A/D and clock interrupts are handled on priority level 6, with the A/D higher in priority (closer to the processor) than the clock. The scope control interrupt is on priority level 4. The priority levels cannot be changed. Since the three interrupt circuits act in essentially the same manner, only the A/D interrupt will be discussed.

Flip-flops FF1A and FF2A start out in the cleared (zero) state, since the interrupt line ADC INT A H has been low. Therefore, E84-3 is high, so that when ADC INT A H goes high (A/D interrupt), BR6 L goes low, requesting an interrupt on priority level 6. Some time later, the interrupt request is granted, and BG6 H goes high. BG6 H is buffered by E91, so that E91-3 goes high. This transition sets FF1A, and

initiates a 100-nsec. delay through E92, Q3, and E83. Before the end of this delay, FF1A (1) H goes high, so that E83-1 holds the bus grant output low at the end of the delay (i.e. the bus grant stops at the interrupting device and is not passed on). If the A/D had not been the interrupting device, FF1A would be held at Ø due to INT A H being low, FF1A (1) H would be low, and at the end of the 100-nsec. delay, the bus grant BG6 would be passed on (IV BG 6 PASS, to the INT B circuitry).

When FF1A is set, since FF2A is still at Ø, pins 8 and 9 of E83 are both high, causing BUS SACK L to go low. This indicates to the processor that the bus grant has been received. The processor then removes the bus grant so that BG6 IN H goes low. This causes a positive transition at E82-12 which sets FF2A.

With both FF1A and FF2A set, E83-13 goes low, asserting BUS BBSY L, indicating that the interrupting device has taken control of the bus. At the same time, E74-6 goes low, which, through E37, enables E95 and E96. This gates the interrupt vector address onto the BUS DØ8:DØ2 lines and asserts BUS INTR L.

The processor responds with BUS SSYN L when it has received the vector. This signal goes through E89 to reset the A INT flip-flop (IV A INT DONE L). This causes ADC INT A H to go low, so that E71-11 goes low, and FF1A and FF2A both are reset. Resetting FF1A and FF2A removes the vector from the bus, disqualifies BUS BBSY L and BUS INTR L, and returns the circuitry to its original state.

The starting interrupt vector may be set in increments of 2Ø up to a maximum of 76Ø, using S2. Vector selection is illustrated in figure 3:

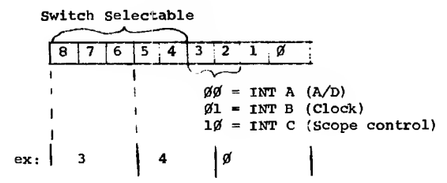


Figure 3: AR11 Vector Address Selection

Location of the vector switches on the module is shown in figure 2. The switches are set "on" for a 1 and "off" for a Ø (note that this is opposite to the address switches), i.e. to set up a vector of 34Ø, bits 7, 6 and 5 are "on" and bits 8 and 4 are "off".

Bits 3 and 2 are gated onto the bus by E96 as a function of which of the three interruptsis active.

4.0 REAL-TIME CLOCK

The real-time clock consists of a free-running 1 MHz crystal oscillator circuit, a series of four decade counter dividers to generate additional frequencies of 100 KHz, 10 KHz, 1 KHz, and 100 Hz, a multiplexer to select a single frequency for input to a counter, and three registers (clock preset buffer, clock counter, and status).

4.1 Crystal Oscillator

The oscillator consists of two 8640 gates, connected as inverters with ac-coupled inputs and resistive feedback in a cross-coupled configuration through the 1 MHz crystal. The crystal acts as a low impedance only at 1 MHz and as a high-impedance at all other frequencies. Consequently, at 1 MHz, the two gates are set up in a cross-coupled configuration and oscillation occurs. The output signal RTS PS CLK, available on TP C, is a clean TTL 1 MHz signal. This signal is used directly as a power supply clock, and gated in E81 by the enable counter signal RTC ENA CNTR (1) L before going to the dividers. When the counter is not enabled (RTC ENA CNTR (1) L is high) the counter output can be simulated by the maintenance signal RTC TEST COUNTER H through E81.

4.2 Divider Chain and Multiplexer

The 1 MHz signal is used to generate 100 KHz, 10 KHz, 1 KHz and 100 Hz signals using 74190 decade up/down counters E98 through E101, running in the upcount mode. Each counter increments on the low-to-high transition of the pin 14 input. The pin 13 output goes low when the pin 14 input is low and the counter state is 9, providing a low pulse to the next stage.

The five crystal-based frequencies generated in this manner go to the multiplexer E97, along with the external input and

auxiliary clock input. One of these frequencies is selected according to the rate select bits (RTC RATE Ø (1) H, RATE 1 (1) H and RATE 2 (1) H) on E97 pins 11, 10 and 9. The selected rate appears in inverted form on the pin 6 output ($\bar{F}$) of the E97 multiplexer. Since the signals from the divider chain are low-going pulses (½ µsec), the signal on E97-6 is a positive pulse. Under normal conditions, E90-7 is high, so that the multiplexer output goes through E90 and appears as a low-going pulse RTC CLK OUT L, which is the input to the clock counter. If BAS MAINT CLK CTR L is low, E90 serves to "stretch" the RTC CLK OUT L pulse, to prevent the counter from changing state while it is being read by the processor.

4.3 Clock Counter and Buffer

The clock counter is an 8-bit presettable counter register consisting of 74193 4-bit up/down counters E40 and E41, used in the upcount mode. Count input is RTC CLK OUT L, on E40 pin 5. Every 16th count, E40-12 propagates the signal into the E41 pin 5 input. The counter register is cleared on INIT, and loaded from the preset register on RTC LD CLK CNTR L, which occurs on overflow in continuous interval mode (mode 1) or when the clock buffer is loaded when the clock is disabled.

The clock buffer register is loaded from the BIO OUT Ø7:ØØ H lines when its address is selected (BAS CLK BUF L goes low). The buffer register load pulse is gated through E71 when the counter is not enabled (RTC ENA CNTR (Ø) H is high), so that the clock counter is also loaded.

In continuous interval mode, RTC CLK MODE 1 L is low (E81-5) so that E81 acts to invert the signal on E81-6. In single interval mode, E81-5 is high so that E81-4 is low and the clock counter is never loaded via E57-12.

In continuous interval mode the low-going overflow pulse RTC CLK OVRFLW L appears at E81-3 and is inverted at E81-1. This high-going pulse is ac-coupled through C7, so that its trailing edge causes a low at E81-6. This causes a high pulse at E81-4 which occurs just after the overflow pulse, and causes the clock counter to be reloaded from the clock buffer register.

The clock overflow signal occurs whenever the counter goes from 377 to Ø. The pulse actually goes low during the 377 state, and its trailing edge corresponds to the 377 to Ø transition. Consequently, the counter is reloaded with the preset value at the beginning of the Ø state.

4.4 Clock Status Register

The clock status register is a read/write register whose bits control the functions performed by the clock. The high byte of

this register consists of one-half of E58 (bit 15) and E75 (bits 8, 11 and 14). The high byte is loaded on a pulse from E57-10, the and function of BAS CLK STAT L and BAS OUT HIGH L. The low byte of this register consists of one-half of E58 (bit 7), one half of E7Ø (bit Ø), and E76 (bits 1, 2, 3 and 6). The low byte is loaded on RTC LD CLK LOW H, E57-4, the and function of BAS CLK STAT L and BAS OUT LOW L.

Bit 15, the external flag, is loaded from BIO OUT 15 H when the register is loaded. It is set by the external signal ADC EXT ST (1) L and reset by BAS B INIT L. Bit 14, part of the 74175 E75, is loaded from BIO OUT 14 H. When bit 14 = 1, E68 is enabled to set the clock interrupt flip-flop E7Ø on the occurrence of the external input ADC EXT ST (1) L. Bit 11, RTC TEST COUNTER H, is used for maintenance purposes to test the clock divider chain. Bit 8, clock mode, determines whether the clock is in continuous interval mode (1) or single interval mode (Ø).

Bits 3, 2, and 1, part of the 74175 E76, are loaded from BIO OUT Ø3:Ø1 H when the low byte of the register is loaded. These bits determine the selected rate according to Table 2. Bit 6, also part of E76, is used by E68 to enable the clock overflow to cause an interrupt.

TABLE 2 - Rate Select

Bit 3 Rate 2	Bit 2 Rate 1	Bit 1 Rate Ø	Frequency
Ø	Ø	Ø	——
Ø	Ø	1	1 MHz
Ø	1	Ø	1ØØ KHz
Ø	1	1	1Ø KHz
1	Ø	Ø	1 KHz
1	Ø	1	1ØØ Hz
1	1	Ø	External
1	1	1	Aux-pin EL2

Bit 7, the clock done flag, is loaded from BIO OUT Ø7 H when the low byte of the register is loaded. It is set by RTC CLK OVFLW L and reset by BAS INIT L. Bit Ø, the clock enable bit, is loaded from BIO OUT ØØ H when the low byte of the register is loaded. It is reset from E69-10, the or function of BAS INIT H and clock overflow in single interval mode, from E69-1.

5.0 ANALOG POWER

The analog power supply is shown on page 8 of the M78Ø9 schematic, labelled HQP (High Quality Power). The power supply is a dc-to-dc converter, which develops ±14V dc (nominal) from the +5V logic supply. Instead of using a step-up transformer, the power supply uses diodes and capacitors in an extension of the basic voltage doubler technique.

5.1 Voltage Doublers

A basic voltage doubler is shown in figure 4. Its input

is a square wave running between ground and +5V. During the time that the input is at ground, diode D1 conducts, and C1 charges to +4.3 volts (+5 volts minus the D1 diode drop). In the next half-cycle, the input is at +5V. Since the voltage across the capacitor C1 remains constant, V_1 goes to +9.3 volts, and D1 becomes back-biased. During this interval, D2 conducts, and V_{out} charges to one diode drop less than V_1, or +8.6 volts.

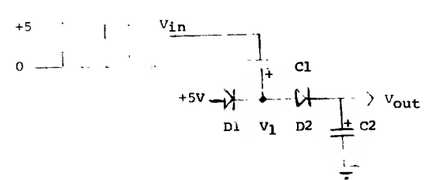


Figure 4: Voltage Doubler

In the next half-cycle, we are back to the beginning, with V_{in} at ground and D1 conducting, charging C1. At this time, V_1 is at +4.3 volts, and D2 is back-biased. The output voltage remains at +8.6 volts, i.e. we have transformed the +5V input to a +8.6 volt output. Note that if we ignore the two diode drops, we have effectively doubled the input voltage. A good way of looking at the process is that the circuit represents a "bucket brigade". During one half-cycle, charge is passed to C1 through D1. During the next half-cycle, charge is then transferred from C1 to C2

through D2. Obviously, if we cascade multiple sections, higher voltages can be attained, as charge is passed in "bucket brigade" fashion from one capacitor to the next and ultimately from the last capacitor into the load.

5.2 Square Wave Driver

The 5V square wave input voltage for the AR11 power supply is produced by transistors Q5 and Q6. Transistor Q5 is a PNP which pulls the voltage up to +5 Volts. Transistor Q6 is an NPN which pulls the voltage down to ground. In such circuits, with both active pullup and active pulldown, it is important to guarantee that the two transistors are never on at the same time, even for an instant during switching. This is especially difficult since in general transistors turn off more slowly than they turn on. In the AR11, to guarantee that one turns off before the other turns on, a full 1-µsec interval is allowed.

The signal RTC PS CLK, a 1 MHz (1 µsec) square wave, is applied to pin 14 of E49, a 7493 divide-by-16 counter. The most significant bit of this counter is applied through E48 to the input of flip-flop E45, whose outputs are squars waves with a 32-µsec. period. During each half-cycle of the 32-µsec square wave, the 7493 E49 counts from Ø to 15, remaining in each state for 1 µsec. The 7420 E37 decodes the 15 state, so that its pin 8 output goes low for the last microsecond of each half cycle. This

causes both the pin 8 and the pin 6 outputs of E56 to go high, so that all the E27 outputs are low. When HQP A L (E27-2) is low, Q4 turns on, thereby turning off Q5. When HQP C L (E27-8, 10, 12) is low, Q6 turns off. Thus for the last microsecond of each half-cycle, both Q5 and Q6 are turned off, allowing the one which had been on to turn off completely before the other turns on. The resulting waveforms are shown in figure 5. Note that the square wave drive signal (TP PD) shows a definite intermediate state at the time when both Q5 and Q6 are off.

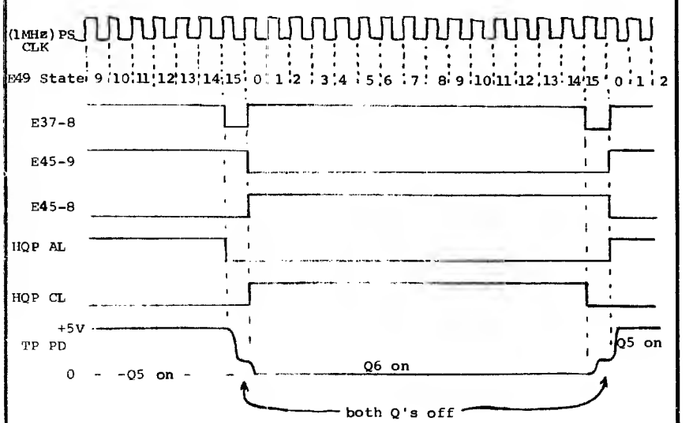


Figure 5: Square Wave Timing Waveforms

5.3 First Stages

The first stage of the power supply "doubler chain" consists of D4 through D9 and C12 through C14. These are driven directly by the output of Q5 and Q6, as seen at TP PD. Since the diode-capacitor chain functions as a "distributed transformer", the early low-voltage stages run at the highest current levels. Consequently, the TP PD voltage is not the idealized zero-to-+5V signal, but actually only exhibits about a 4.5V swing. The diodes (even though doubled up) exhibit a drop of roughly .85 volts. By the analysis of section 5.1, this results in +7.3 volts dc at the positive end of C13. When TP PD is low, this results in 7.3 - .85 = 6.45 volts at the cathode of D8 and D9. When TP PD goes high, we get 6.45 + 4.5≈11 volts at the cathode of D8 and D9. Referring to figure 4, TP PD is high when HQP A L is high. At this time HQP BL is also high, so that Q7 is off, allowing Q8 to be turned on. In the opposite half-cycle, HQP B L is low, turning on Q7 and thereby turning off Q8. Meanwhile E27-6 goes high allowing Q9 to turn on. This results in a ≈10 Volt square wave at the collectors of Q8 and Q9. As in the case of TP PD, the collectors of Q8 and Q9 exhibit the 1-μsec intermediate state, when both transistors are off.

5.4 Output Stages

The ≈10V square wave at the collectors of Q8 and Q9 is the input signal for the output diode-capacitor chains. By following an analysis similar to that of section 5.1, allowing roughly .75 Volts for each diode drop, but ignoring the effect of zener diodes D13 and D14, output voltages in the range of ±16 Volts to ±17 Volts are arrived at, which would be somewhat higher than desired. However, zener diodes D13 and D14 (whose nominal values add to 15V) act as a regulating negative feedback loop. As the minus supply becomes more negative than -14 Volts, the zeners begin to turn on. This "steals" base drive current from Q9 when it is on, keeping Q9 out of hard saturation and thereby dropping the magnitude of the Q8-Q9 output square wave. This negative feedback loop automatically adjusts the square wave voltage so as to maintain the negative output near -14 Volts. Since the positive supply is also based on the same square wave, it also ends up near +14 Volts.

The two outputs are "smoothed" by LC filters (L2-C25, C24 on the minus side; L1-C21, C23 on the plus side) with a break frequency of roughly 4 KHz, which tend to reduce the ripple and remove high frequency components present due to the switching transients.

The M78Ø9's digital and analog grounds are connected in the middle layer at a single point near the return (ground) end of

these filter capacitors.

6.0 ANALOG BIAS CURRENT SOURCES

All analog circuitry in the AR11 is biased by means of current sources, in order to be immune to variations in power supply voltage. The current sources are all shown on page 9 of the M78Ø9 schematics, ABS (Analog Bias Sources).

The reference upon which all the current sources are based is D49, a 1N825 6.2V reference zener diode. This zener is specified to have minimum thermal drift when run at a current level of 7.5 mA. A simplified version of ABS is shown in figure 6, in which Q14 through Q19, Q28 and Q29 have been combined as a single transistor Q_A, and Q25 through Q27 and Q74 have been combined as Q_B.

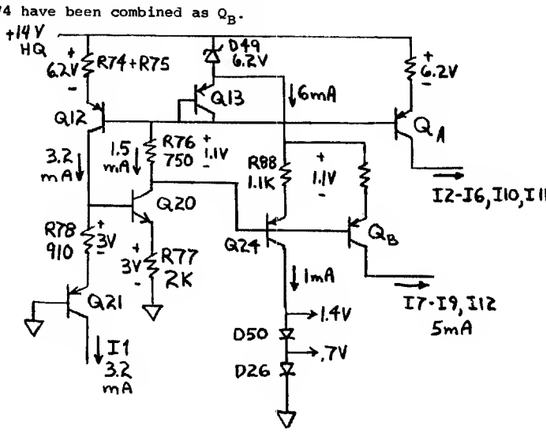


FIGURE 6: SIMPLIFIED ABS

In analyzing this circuit, we start at zener diode D49, and assume that it is operating at 6.2Volts, its nominal value. Transistor Q13 has base and collector tied together, so that its base-emitter (b-e) junction acts as a diode. Since the Q13 b-e drop matches the b-e drop of Q12, there is also 6.2 Volts across R74 and R75. Potentiometer R75 is adjusted so that I_e = 6.2/(R74 + R75) = 3.2 mA≈I_C. Consequently, the collector of Q12 is a 3.2 mA current source, as shown in figure 5. This current goes through R78 and Q21 and appears as I1 at the collector of Q21. Along the way, it sets up a 3 Volt drop across the 910-ohm R78. Since the b-e drops of Q21 and Q20 match, we also have 3 Volts across the 2K R77. This causes the collector of Q20 to be a 1.5 mA current source. This 1.5 mA comes down from the positive supply through the reference zener D49, Q13, and R76. The 1.5 mA through the 750-ohm R76 establishes a 1.1 Volt drop across R76. Since the b-e drop of Q13 matches those of Q24 and Q_B, we also have 1.1 Volts across the emitter resistors of Q24 and Q_B. With an emitter resistor (R88) of 1.1K, Q24 becomes a 1 mA current source. This 1 mA goes to ground through D26 and D50, thereby setting up voltages of .7 Volts and 1.4 Volts for use on pages 11 and 12 of the M78Ø9 schematics. Likewise, the 1.1 Volts across the emitter resistor of Q_B (actually R89, R90, R91, R105) sets up current sources I7, I8, I9, and I12, which total 5 mA. This 5 mA, the 1 mA in Q24, and the 1.5 mA in Q20, combine to make the desired

7.5 mA in D49, the reference zener. Since the Q13 b-e drop matches the b-e drop of Q_A we have 6.2 Volts across the emitter resistor of Q_A (actually R83 + R171, R84 + R172, R85 + R173, R86 + R174, R87, R92, R93). This sets up current sources I2, I3, I4, I5, I6, I10 and I11.

7.0 SCOPE CONTROL

The scope control circuitry is shown on four pages of the M78Ø9 schematic: p. 13 DIR (Display Registers), p. 14 DIL (Display Logic), p. 15 DACX and p. 16 DACY. Since the X and Y D/A converters are identical, only the X D/A converter will be described.

7.1 DIR (Display Registers)

The X Buffer Register consists of 74175 E7 (bits 6-9)and 74174 E8 (bits Ø-5). It is loaded from BIO OUT Ø9:ØØ H on DIL LD X BUF H, which originates on the display logic page. It is cleared on BAS INIT L.

The Y Buffer Register consists of 74175 E1 (bits 6-9) and 74174 E2 (bits Ø-5). It is loaded from BIO OUT Ø9:ØØ H on DIL LD Y BUF H, and cleared on BAS INIT L.

Since the 74174 IC has its outputs available only in (1) H form, 7404 hex inverters E3 and E9 are employed to provide Y5 through YØ and X5 through XØ in (1) L form for use by the D/A converters.

Display Status Register bits 9-11 are contained in 74175 E13.

They are loaded from BIO OUT 11:Ø9 H on DIL LD DISP HIGH H, and cleared on BAS INIT L. Bits 9, 10, and 11 are CHØ2 STORE, and WRITE THRU. CHØ2 H is inverted by open collector inverter E15, pulled up to +5V by R115 and output through J1-B as CHØ2 L. STORE (1) L is inverted by E15 and output through J1-E as NON STORE L (note the inversion). WRITE THRU H is inverted by E15 and output through J1-A as WRITE THRU L.

Display Status Register bits 2, 3 and 6 are contained in 74175 E14. They are loaded from BIO OUT Ø2, Ø3 and Ø6 H on DIL LD DISP LOW H, and cleared on BAS INIT L. Bits 2 and 3 are DIR DISP MODE Ø (1) H and MODE 1 (1) H, used on the display logic page to control the intensification mode. Bit 6 is DIR DISP INT ENA (1) H, used on the display logic page to enable an interrupt upon completion of intensification of a point.

7.2 DIL (Display Logic)

The display logic page contains scope intensification circuitry, storage scope, erase controls, ready (done) bit, interrupt control, and gates which generate load pulses for the various display registers.

On the left side of the page, the load pulses are generated by E19 and E24, using the register select and output byte signals from the BAS (Bus Address Select) page.

A scope intsnsification pulse is generated (after appropriate delay) under the following conditions:

INTENSIFICATION MODE	BIT 3 MODE 1 (1) H	Bit 2 MODE Ø (1) H	CONDITION
Ø	Ø	Ø	Set bit Ø
1	Ø	1	Load X
2	1	Ø	Load Y
3	1	1	Load X or Load Y

TABLE 3: Intensification Modes

These conditions are decoded by 7453 E20. For example, if we are in mode 2, MODE 1 (1) H is high, so that when we get LD Y BUF H (load Y buffer register) pins 1 and 13 of E20 are both high, and pin 8 goes low. The low on E20-8 causes a high on E15-2 which causes two things to happen: the signal causes a low on E19-10, which resets E25, the ready (done) flip-flop. It also fires one-shot E21. The resultant E21 delay is to provide time for the D/A outputs and scope beam to settle before intensifying the point on ths scope. The E21 delay is nominally 20 µsec, but can be set to 80 µsec for slow storage scope applications by connecting W3. At the end of the E21 delay, a low-to-high transition occurs on E21-4, which fires the other one-shot in E21. This one-shot determines the intensification pulse duration-nominally 2 µsec, but jumperable to 6 µsec for slow storage scopes by means of W6. Either the high or low output of the second one-shot can be applied to E15-13 as a function of whether W4A or W4 is connected, depending on whether a high or low intensification

pulse is desired. After the E15 inversion, the pulse is applied to the base of Q51, which amplifies and re-inverts the pulse for output to the scope. Q52 acts as a 20 mA current source pullup for the output pulse. The output pulse is clamped at 3.3 Volts by zener diode D32, or at 1.4 Volts by diodes D33 and D34 if W5 is connected. The high-going intensification pulse from E21-5 passes through E19 and sets the ready (done) flip-flop E25 on its trailing edge.

Bit 12 of the Display Status Register is implemented by the erase flip-flop E23. It is loaded from BIO OUT 12 H on the DIL LD DISP HIGH H pulse. Setting the Erase flip-flop initiates two actions: ERASE (1) H resets the ready (done) flip-flop E25 through E19, and the inverted (through E15) erase signal DIL ERASE L is applied to the external storage scope through J1-C. The storage scope responds with a low signal ERASE RET L on J1-H. This turns off Q53, so that DIL ERASE CLR H is pulled up to +5V through R121. ERASE CLR H goes through E24 and resets the Erase flip-flop E23 through pin 1. After the interval of time necessary to erase its screen (typically one-half second), the storage scope brings ERASE RET L back to a high voltage level. This turns on Q53, bringing DIL ERASE CLR H low. The resulting low-to-high transition on E19-13 sets the ready (done) flip-flop E25.

When DIR DISP INT ENA (1) H is high, the display interrupt is enabled. In this case, setting the ready (done) flip-flop

as a result of either an intensification pulse or completion of an erase operation, sets the display interrupt flip-flop E25. The resulting interrupt signal DIL INT C H is processed by the IV circuitry. Upon completion of the interrupt, IV DISP INT DONE H resets E25 through E24. Both the erase and interrupt flip-flops are also reset by BAS INIT H, acting through E24.

7.3 D/A Converters

The following description applies to both the X and Y D/A converters, which are identical. Designations of components and signal names apply to the X D/A, page 15 of the M78Ø9 prints.

The D/A converter consists of a 10-bit converter with high output impedance (about 8K) plus a buffer amplifier to lower the output impedance and provide the current needed to drive the capacitive load of the cable to the scope.

7.3.1 Converter

The converter consists of an 8-bit current-output IC D/A (bits Ø-7), two discrete component higher-order current sources (bits 8 and 9) and an offsetting current source I4 (.625 mA), working in conjunction with precision resistors R148, R140, R141 and R145 to give a ±5 Volt output.

The IC D/A E10 is powered from DACX +5V HQ, which is the +5 Volt power line filtered by L3 and (C34 + C35). Reference current for this D/A is ABS I2-3.27 mA, running into pin 13.

Consequently, its full scale output current (all logic inputs-pins 5 through 12 - high) is 3.27 mA. Resistance seen by this output current is R145 - 768 ohms. Consequently, bits Ø-7 have a total weight of (3.27 mA) (768 ohms) = 2.5 Volts, or one-quarter of full-scale.

Now let's examine the two high-order current sources. Assume that X9 (1) L and X8 (1) L are both high, so that E16-2 and -12 are low, and therefore Q54 and Q55 are both off. Voltage reference ABS VB2 is set up on the ABS page-it is 4 Volts plus one transistor b-e drop above the -14V HQ supply. Consequently, the emitters of Q58 and Q59 are 4 Volts above the -14 VHQ supply. It is important to note that this voltage tracks along with the negative supply, so that the voltage across (R136 + R139) and across (R137 + R138) is a constant 4 Volts, independent of the exact level of the negative supply voltage. The values of (R136 + R139) and (R137 + R138) are adjusted so that 1.25 mA current flows in the output line of each current source. Because of the high-current-gain complementary NPN-PNP configuration, Q58 and Q59 base currents are negligible. The 1.25 mA output current from the bit 8 source (Q59, Q57) sees a resistance of (R141 + R145), approximately 2K. Consequently bit 8 has a weight of (1.25 mA) (2K) = 2.5 Volts, or one quarter of full-scale. The 1.25 mA output current from the bit 9 source

(Q58, Q56) sees a resistance of (R140 + R141 + R145), approximately 4K, so that bit 9 has a weight of (1.25 mA)(4K) = 5V, or one-half of full-scale.

Assume an all 1's (1777) input to the D/A. DIR X9 (1) L and X8 (1) L are now low, so that E16-2 and -12 are high, and Q54 and Q55 are on. In this case, the Q54 and Q55 emitters clamp at +.7 Volts, leaving 4.3 Volts across R130 and R131. Q54 and Q55 become current sources, with a value I = (4.3V/3K) = 1.43 mA.

Since this current is greater than 1.25 mA, all the current from (R136 + R139) and (R137 + R138) is "stolen", Q58 and Q59 turn off, and the bit 9 and bit 8 currents are zero. Since the input is all 1's, E10-5 through -12 are all low, so that the E10-4 output current is also zero. This leaves only I4-.625 mA flowing. I4 goes to ground through (R148 + R140 + R141 + R145), approximately 8K. Consequently, the voltage at the base of Q61 during the 1777 condition is (.625 mA) (8K) = +5 Volts.

If we go to all Ø's, Q54 and Q55 turn off, allowing the 1.25 mA bit 8 and bit 9 current sources to turn on. E10-5 through -12 are now all high, so that the E10-4 output current is 3.27 mA. These sum up linearly, giving a voltage (as seen at the base of Q61) of +5V (due to I4) -5V (due to bit 9) -2.5V (due to bit 8) -2.5V (due to bits Ø-7) = -5 Volts

Note that the all Ø's case, with -5 Volts output, actually represents all bit currents on, and the all 1's case, with +5 Volts output, actually represents all bit currents off, with only the offset current I4 on. Since the circuit is linear, any digital combination between ØØØØ and 1777 results in the proper corresponding voltage between -5 Volts and +5 Volts.

The impedance seen at the base of Q61 is the sum of R148 + R140 + R141 + R145, or 8K. If WX is shorted, this 8K is now in parallel with (R134 + R135) = 886 ohms, for a resulting equivalent resistance of 800 ohms. Since this is exactly one-tenth of the original 8K, shorting WX has resulted in one-tenth the output voltage range, or ±.5 Volts. Connecting a resistor in place of WX can result in any resistance desired between 8K and 800 ohms, and therefore in any voltage range desired between ±5 Volts and ±.5 Volts.

7.3.2 Buffer Amplifier

The voltage seen at the base of Q61 has 8K source impedance, and is therefore unsuitable for output drive. To provide output drive, a buffer amplifier consisting of Q61, Q62 and Q63 is provided.

Bias current for this buffer amplifier is I10, a 1 mA current source. If the input voltage (Q61-base) equals the

output voltage (Q62-base), I10 splits equally and ½ mA shows up in the collector of both Q61 and Q62. The Q61 collector current goes through D38 and R142 to the minus supply. Since the D38 diode matches the Q63 b-e drop and R142 and R143 have equal values, the Q63 collector current equals the Q61 collector current. For equal split of I10 between W61 and Q62, we therefore, have the current out of Q62 equal to the current into Q63, so that there is no net current into or out of C33. This gives us a stable output voltage. If the Q61-base voltage is lower than the Q62-base voltage, more of I10 goes through Q61 than Q62, so that the Q63 current is higher than the Q62 current and we have a net current flow out of C33. Consequently, the C33 voltage (which is also the voltage on the base of Q62) drops, until the Q62-base voltage equals the Q61-base voltage, at which point I10 again splits equally and a stable condition is reached. In this manner, the output voltage (Q62-base) follows the input voltage (Q61-base). Output impedance of this amplifier is approximately 50 ohms. The 47-ohm protection resistor R144 brings the output impedance up to 100 ohms. The Q61 and Q62 b-e junctions are protected for large steps by diodes D35 and D36. The amplifier is protected from "outside-world" overvoltages by fusible resistor R144 and diodes D37 and D39.

8.0 A/D CONVERTER

The A/D circuitry is contained on three pages of the M78Ø9 schematic: page 10, ADC (A/D Control), which contains all the A/D logic; page 11, ADCS (A/D Channel Select), which contains the input protection circuitry and analog multiplexer; and page 12, AD (A/D), which contains the sample-and-hold circuit and the actual A/D converter.

8.1 A/D Control

The A/D Status Register high byte is contained in 74174 E63. It is cleared on BAS B INIT L, and loaded from BIO OUT 13, 11:Ø8 H when the A/D Status Register and a high byte output operation are selected. The four-bit channel address and unipolar/bipolar bit are contained in the high byte of the status register.

The A/D Status Register low byte is contained in 74175 E77. It is cleared on BAS B INIT L, and loaded from BIO OUT Ø6:Ø4 H when the A/D Status Register and a low byte output operation are selected. Bit 6 is used to enable an interrupt on setting of the A/D done flag. Bit 5 enables an A/D conversion to start on overflow from the real-time clock. Bit 4 enables an A/D conversion to start on an external input.

Bit Ø of the A/D Status Register is used for a program-controlled A/D conversion start. The A/D Status Register low byte load pulse goes through 7404 inverter E48 to one-shot E34. This one shot triggers on the register load pulse if BIO OUT ØØ H is

high, i.e. if a "1" is being loaded into the A/D Status Register bit Ø. The one-shot time is nominally 8 µsec., which is long enough to allow for the analog multiplexer to settle to its new value before signalling the sample-and-hold to hold the signal, at which point the conversion begins. If it is desired to switch between bipolar and unipolar channels, a 7.5 Volt inter-channel difference is possible instead of the normal maximum of 5 Volts. In this case, W1 is connected, lengthening the one-shot time to 11 µsec, which is sufficient for the 7.5 Volt difference.

At the end of the E34 delay, E34-12 goes high, setting the E44 "Hold" flip-flop, which commands the sample-and-hold circuit to hold the analog value for conversion. At the next occurence of the HQP AD CLK H low-to-high transition (which could be anywhere from 0 to 2 µsec later), the E44 "Enable A/D" flip-flop is set, which signals the AM2504 successive approximation register (SAR) E26 to begin the A/D conversion. The SAR then sequences through the ten A/D bits, for each bit making its logical decision on the low-to-high transition of HQP AD CLK H, as a function of ADC COMP L. The AD CLK is a 2-µsec clock signal derived from the 1 MHz crystal oscillator by the E49 power supply counter. Consequently, it takes two microseconds for each "bit decision". The decision signal (COMP L) is derived from the output of the comparator (AD COMP H) by 7405 inverter E47. By jumpering AD COMP H (TP1) to ground, it is possible to bypass the analog circuitry

and simulate that comparator output which results in a 1777 conversion. By jumpering ADC COMP L (TPØ) to ground, it is possible to bypass the analog circuitry and simulate that comparator output which results in a ØØØØ conversion.

After the least significant bit (ADØØ) has been resolved, ADC EOCP L goes low, so that E47-2, 6 are pulled high by R35. After one microsecond, HQP AD CLK H goes low, so that E47-2, 6 are pulled low by E47-2. This causes a low-to-high transition on E48-8, which loads the A/D Buffer Register (E39 and E43) with the converted value information contained on the SAR outputs AD ØØ:Ø9 H.

ADC EOCP L is inverted by E48 to create ADC EOCP H. This is or'ed with BAS INIT H in E46 to create ADC CLR L. This signal resets the "Hold" and "Enable A/D" flip-flops to their original (Ø) states, and is input to SAR E26-14. This signal is present for two microseconds, until the next low-to-high transition of HQP AD CLK H, which then resets the SAR E26.

Bit Ø of the A/D Status Register is held at "1" throughout the 8-µsec A/D Start delay and the conversion interval by or-gate E28, which creates ADC AD STAT ØØ (1) H from HOLD (1) L and the output of the 8-µsec A/D Start delay one-shot.

ADC EOCP H also sets the "AD DONE" flip-flop E45 on its leading edge. Its output ADC AD DONE (1) H is used as bit 7 of the A/D Status Register. When an A/D interrupt is enabled,

ADC AD INT ENA (1) H is high, so that setting the "AD DONE" flip-flop causes E56-11 to go low and E48-4 (ADC INT A H) to go high. This causes the A/D interrupt. When the interrupt is complste IV A INT DONE L goes low. This causes E56-3 to go high and E46-10 to go low, thereby resetting AD DONE. If the A/D interrupt is not enabled, AD DONL is not reset until a read operation is psrformed on the A/D Buffer Register. When this occurs, BAS IN L and BAS AD BUF L both go low, so that E46 goes high and E46-10 goes low, thereby resetting the "AD DONE" flip-flop. This flip-flop is also reset by BAS B INIT L, acting through E56 and E46.

An A/D conversion may also be started by either an external start signal or a clock overflow. The external start signal (J1-U) high-to-low transition fires one-shot E34 to create a 500-nsec ADC EXT ST (1) pulse. ADC EXT ST (1) L is used as the external input by the real-time clock counter. ADC EXT ST (1) H is used by the real-time clock for its external interrupt and by the A/D for external starts. If the A/D external start is enabled, ADC EXT ENA (1) H is high, and ADC EXT ST (1) H on E68-3 causes E68-6 to go low, thereby setting the "HOLD" flip-flop and initiating the conversion sequence. If the clock overflow start is enabled, ADC AD CLK ENA (1) H is high, so that RTC CLK OVFLW H on E68-4 causes E68-6 to go low, thereby setting HOLD and initiating the conversion sequence.

8.2 A/D Analog Block Diagram Description

The AR11 uses a unique auto-zeroing A/D configuration, in which the same amplifier front end is shared between the eample-and-hold and A/D comparator is such a manner as to cancel out its own offset and drift.* This configuration is shown in figure 7.

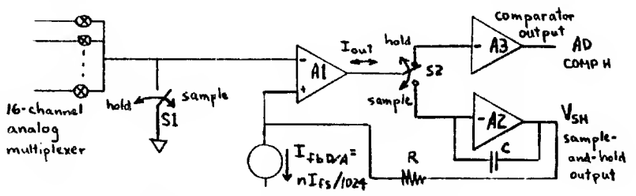


FIGURE 7: A/D Analog Block Diagram
*patent pending

Amplifier A1 is the front end which is shared between the comparator and sample-and-hold. This amplifier is an operational transconductance amplifier, i.e. its input stage is that of an ordinary operational amplifier, but its output is a current source I_{out} instead of a voltage source.

First let's consider the tracking, or "sample" mode of operation, in which S1 is open, S2 is down, and the feedback current source is off, i.e. $I_{fbD/A}$ = 0. Under these conditions, A1 output current I_{out} is integrated and converted to a voltage by sample-and-hold output stage A2, so that the A1-A2 combination acts like an operational amplifier. The A2 output is fed back

to the A1 input, so that the A1-A2 op amp is in a follower configuration, with the A2 output voltage tracking the selected analog input present on the inverting A1 input.

When it is time to do an A/D conversion, S2 switches from the down to the up position on setting of the "HOLD" flip-flop. This leaves integrator A2 with zero input, so that feedback capacitor C holds the A2 output voltage constant. This will now serve as the A/D input voltage. On setting of the "ENABLE AD" flip-flop zero to two microseconds later, the 16-channel analog multiplexer is disabled, so that the selected channel switch opens up, and S1 closes, putting a ground reference on the inverting input of A1. Under these conditions, A1 serves as the comparator input stage. A1 output current I_{out} is converted to a logic-compatible voltage level AD COMP H by output stage A3. Ths successive approximation logic now looks at AD COMP H and proceeds to find that value of n ($Ø \leq n \leq 1Ø23$) which results in zero input to amplifier A1. This occurs at $I_{fbD/A} = n\, I_{FS}/1024 = V_{SH}/R$; $n = 1024\, V_{SH}/RI_{FS}$. If we set the scaling such that $RI_{FS} = V_{FS}$, the desired full-scale input voltage, we have $n = 1024\, V_{SH}/V_{FS}$. During "sample", V_{SH} was tracking the input voltage V_{in}, i.e. $V_{SH} = V_{in}$. Consequently, $n = 1024\, V_{in}/V_{FS}$, which is the desirsd A/D relationship. For V_{FS} = 5 Volts, input voltages of 0 to 5 Volts (1023/1024) result in conversions of Ø to 1Ø23, i.s. ws havs a unipolar input range.

Now assume identical conditions in "sample" mode except that instead of $I_{FbD/A} = 0$ we turn on the most significant bit (MSB) so that $I_{FbD/A} = I_{FS}/2$. Under these conditions, V_{SH} tracks the selected input voltage with an offset of $RI_{FS}/2 = V_{FS}/2$. If V_{FS} = 5 Volts, $V_{SH} = V_{in} + 2.5$, so that an input range to -2.5 to +2.5 corresponds to V_{SH} = 0 to +5 Volts. By turning on the MSB during "sample" we have transformed the unipolar input range into a bipolar input range, with the MSB of the feedback D/A acting as its own bipolar offset reference source. The unipolar/bipolar bit of the A/D Status Register controls the input range by controlling the state of the MSB during "sample".

8.3 ADCS (A/D Channel Select)

Page 11 of the M78Ø9 schematic, ADCS (A/D Channel Select) contains the 16-channel analog multiplexer and switch S1 shown in figure 7 above.

Each of the 16 analog input channels comes in through a 1K fusible resistor, which works in conjunction with the diodes of E5 and E11 to protect the AR11 analog multiplexers from input overvoltage conditions. The 16-channel multiplexer consists of two eight-channel PMOS multiplexer IC's E6 and E12. Each of these has three address lines AØ:A2 which select one of eight switches, plus an enable line OE which enables the selected switch when high and turns off all switches when low.

Switch S1 of figure 7 is implemented by FET Q11. During "sample", ADC ENA A/D (1) L is high, so that E18-12 is low and Q10 is off; R72 pulls the gate of Q11 down to -14V HQ and Q11 is off. When it is time to do a conversion, ADC ENA A/D (1) L goes low, E18-12 goes high, and Q10 turns on, with an emitter current of 12 Volts/20K = .6 mA. This current comes out the Q10 collector and turns on D15, so that Q10-C clamps at +.7 Volts. The gate of Q11 is at ground because of the D45 diode drop, so that Q11 turns on, bringing ADCS MUX NODE to ground. This provides a zero reference for A1 (of figure 7) during the conversion.

ADC ENA A/D (1) L also goes to E28-10, 12, causing E28-8, 11 to go high and E18-2, 4 to go low. Thus both ADCS AD MUX Ø ENA H and MUX 1 ENA H are low and both multiplexers (E6 and E12) are disabled during the conversion. This allows Q11 to ground ADCS MUX NODE without having to sink any current except the bias current of A1.

During "sample", ADC ENA A/D (1) L is high, so that E28 pins 9 and 13 are enabled. This allows address bit ADC AD MUX Ø3 H to select which of the two multiplexers is enabled - E6 is enabled on MUX Ø ENA H when AD MUX Ø3 H is high, E12 is enabled on MUX 1 ENA H when AD MUX Ø3 H is low.

The three low-order address bits ADC AD MUX ØØ:Ø2 H are inverted by E18 to provide the address MUX AØ:A2 L to the multiplexer IC's E6 and E12. Since E6 and E12 are PMOS chips, their

logic thresholds are referenced to the +14V HQ supply. Therefore MUX AØ:A2 L, AD MUX Ø ENA H, and AD MUX 1 ENA H are all 14V logic swings, implemented by open collector inverters in E18 and 20K pullup resistors to +14V HQ.

8.4 AD (Converter and Sample-and-Hold)

Page 12 of the M78Ø9 schematic (AD) contains the feedback D/A converter and the following circuits from figure 7: operational transconductance amplifier A1, sample-and-hold output amplifier A2, comparator output stage A3, and switch S2.

The feedback resistor R of figure 7 is actually made up of R109 and R111. The feedback D/A converter is made up of an integrated circuit 8-bit current output D/A E22 and two higher-order discrete component bits, which function in the same manner as described in the D/A converter section. The two higher-order current sources are both nominally equal to 4 Volts/1.25K = 3.2 mA. The MSB (bit 9) current source "sees" the total resistance R109 + R111, approximately 800 ohms, so that its value is 2.5 Volts, or one-half of full-scale. The bit 8 current source "sees" only R111, approximately 400 ohms, so that its value is 1.25 Volts, or one-quarter of full-scale.

During "sample", ADC ENA AD (1) L is high, so that ADC UNIPOLAR H on E17-9 controls the level of E17-10. Since the SAR (E26) was reset at the end of EOCP on the previous conversion, ADC ADØ9 H is high, and E17-13 is high for unipolar and low for

bipolar. When E17-13 is high, Q30 is on so that the R99, R101 current is "stolen" from Q37 and the MSB current source is off. For bipolar range, E17-13 is low, Q30 is off, and the MSB current source is on during "sample", providing the needed half-scale offset. During "sample" AD ENA AD H is low, so that E17-4 is high, Q31 is on, and the bit 8 current source is off. During the conversion, the bit 9 and bit 8 current sources are controlled by ADC ADØ9 H and ADC AD Ø8 H from the SAR, acting through E17. When AD Ø9 H and AD Ø8 H are high, the corresponding current sources are on.

The reference current for E22 is ABS I1 - 3.2 mA. Consequently the E22-4 full-scale output current is 3.2 mA, which is present for E22-5 through -12 all high, i.e. ADC ADØ7:ØØ H from the SAR E26 all "1".

During "sample", ADC ENA A/D (1) L is high, so that E17-1 is at ground. This turns on Q32, so that the gates of Q60 and Q70 are at +14V HQ. Therefore Q60 and Q70 are off and the E22 output current is diverted into D48, so that the bit Ø-7 current is effectively off. During the conversion ENA A/D (1) L is low, E17-1 is high, Q32 is off, and Q60 and Q70 are held on by R96 between gate and source. The E22 bit Ø-7 output current then goes through Q60 and Q70, D18 and D19, and "sees" R111, approximately 400 ohms, so that its value is (3.2 mA)(400 ohms) or 1.25 Volts, which is the desired one-quarter of full-scale.

Operational transconductance amplifier A1 is made up of Q35, Q36 and Q40, biased by current source ABS I6-2 mA. If the base voltages of Q35 and Q36 are equal, I6 will split up with 1½ mA going into Q35 and ½ mA going into Q36, due to the unbalanced emitter resistors R106 and R107. The 1½ mA current from the collector of Q35 is "reflected" by Q40, because the D27 diode drop matches the Q40 b-e drop and R112 and R113 are equal in value. Since the Q36 collector is sourcing ½ mA, and Q40 is sinking 1½ mA, there is a net 1 mA current flowing in the direction from the Q46, Q47 emitters into the Q36, Q40 collectors. This is balanced by the 1 mA current source ABS I8, which flows down through Q44 and Q47 during "sample" and through Q43, Q45 and Q46 during "hold". The difference between this nominal 1 mA and the actual Q36, Q40 current, due to a non-zero Q35-Q36 base difference voltage, acts as the error current into sample-and-hold output stage A2 (Q49, Q50, C28) during "sample" and into comparator output stage A3 (Q48) during "hold".

Switch S2 of figure 7 is actually the current switching network consisting of Q41 through Q47. If ADC HOLD (1) L is high, the circuit is in the sample state. In this condition the bases of Q41 and Q43 are at +5 Volts. The bases of Q42 and Q44 are at +3 Volts, set up by I12-1.5 mA and the 2K pot R114. Since the Q44 base voltage is lower than the Q43 voltage, Q44 is on and I8 takes the right-hand path. Since the Q42 base voltage is lower

than the Q41 voltage, Q42 is on and I7-.5 mA goes down into R117 instead of R116. Therefore the base of Q47 is higher than the base of Q46, and Q47 is on, allowing I8 to continue on into the A1 output. During "hold", HOLD (1) L is low, so that the Q41, Q43 base voltage is +1.4 Volts. Since the 3-Volt Q42, Q44 base voltage is now higher, I7 and I8 take the left-hand paths, through Q41 and Q43 respectively. Common base stage Q45 transmits the I8 current from Q43 on into Q46, which is now on instead of Q47 because I7 is now going into R116 instead of R117.

During "hold", diodes D28 and D29 and transistor Q45 form a feedback path for amplifier A3 (Q48) clamping the comparator output AD COMP H at +2 Volts high and +.8 Volts low.

8.5 Successive Approximation Waveforms

The AR11 A/D converter uses a successive approximation algorithm in which, initially, all ten bit current sources are on. The current sources are then turned off one at a time (MSB first), and after a two-microsecond settling time, a decision is made (on the basis of all the remaining current sources which are still on) as to whether to leave the current source off or to turn it back on. At the "decision time", if the approximation voltage (TP A) is below zero, the bit current source in question is left in the off state, and a "Ø" results; if the approximation voltage (TP A) is above zero, the bit current source in question is turned

back on, and a "1" results. Negative voltage at TP A results in AD COMP H at +2 Volts; positive voltage at TP A results in AD COMP H at +.8 Volts. The approximation voltage (TP A) is a staircase with both plus and minus steps, "zeroing in" on a threshold voltage near zero. Each of the ten steps has one-half the magnitude of the previous step.

DIGITAL EQUIPMENT CORPORATION
MAYNARD, MASSACHUSETTS

ENGINEERING SPECIFICATION DATE 9/30/74

TITLE AR11 Troubleshooting Procedure

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE

TABLE OF CONTENTS

ENG	APPD	SIZE	CODE	NUMBER	REV
Jesse Lipcon 10/1/74		A	SP	AR11-Ø-6	

DEC 16-(392)-1075-N971
DRA 107

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AR11 Troubleshooting Procedure

1.0 SCOPE

This document covers troubleshooting procedures for the AR11 one-module real-time analog subsystem. The AR11 consists of 16-channel 10-bit A/D converter with sample-and-hold, scope control with two 10-bit D/A converters and the associated logic, and programmable real-time clock. Since the AR11 is an SPC Unibus Option, it also contains a Unibus interface. Since the AR11 draws power only from the +5V logic power supply, it also contains a dc-to-dc converter to supply ±14V power for the analog circuitry.

2.0 RELATED DOCUMENTS

The following material should be referenced when using this document:

2.1 AR11 User's Guide DEC-11-HARUG-A-D

2.2 M7809 (AR11) circuit schematics D-CS-M78Ø9-Ø-1*

2.3 AR11 System Installation/Acceptance Procedure A-SP-AR11-Ø-4*

2.4 AR11 Circuit Descriptions A-SP-AR11-Ø-5*

2.5 AR11 Diagnostic Listings

2.5.1 AR11 Test I (Logic) MAINDEC-11-DZARA-A

2.5.2 AR11 Test II (Analog) MAINDEC-11-DZARB-A

2.5.3 AR11 Test III (Wraparound) MAINDEC-11-DZARC-A

2.5.4. DEC/X11 Exerciser Module MAINDEC-11-DXARA-A

2.6 Manufacturer's manual for XY display scope or storage scope being used with the AR11.

*Included in AR11 customer print set

SIZE	CODE	NUMBER	REV
A	SP	AR11-Ø-6	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 2 OF 15

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AR11 Troubleshooting Procedure

3.0 AR11 MAINTENANCE PHILOSOPHY

The AR11 logic is to be repaired in the normal manner. The AR11 analog circuitry is to be repaired only in the AR11 option area. If any analog failures occur either in system integration (FA & T) or in the field, the AR11 is to be board-swapped and returned to the option area for repair. Likewise, no analog adjustments are to be attempted in FA & T or in the field. All potentiometers are sealed after final adjustment in the option area, and from then on are considered to be fixed resistors. All AR11's have been burned in to assure the reliability necessary for successful implementation of this board-swap maintenance philosophy.

It is the intent of this procedure and of the AR11 diagnostics to provide the tools necessary to troubleshoot and repair all digital logic problems, to verify analog performance, and, if A/D or D/A problems are detected, to isolate the problem to either the digital or analog circuitry so that a decision can be made whether to repair the board (digital problem) or to board-swap and return to the option area (analog problem). Field (and FA & T) repairs may be made on the dc-to-dc converter (analog power supply).

4.0 DESCRIPTION OF DIAGNOSTICS

4.1 AR11 Test I (logic) MAINDEC-11-DZARA-A

This diagnostic does a complete checkout of all AR11 logic - Unibus interface, interrupts and vectors, real-time clock,

SIZE	CODE	NUMBER	REV
A	SP	AR11-Ø-6	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 3 OF 15

ENGINEERING SPECIFICATION [redacted] CONTINUATION SHEET

TITLE AR11 Troubleshooting Procedure

A/D logic, D/A and scope control logic.

The diagnostic is set up to automatically test multiple AR11's installed in a system provided that the following conditions are met: first (or only) AR11 address 77Ø4ØØ, vector 340; additional AR11's 2Ø higher and sequential, e.g. 77Ø420 and 36Ø, 77Ø44Ø and 4ØØ, etc.; address which is 2Ø higher than the last AR11 address must be unused, e.g. 77Ø42Ø in system with one AR11, 77Ø46Ø in system with three AR11's. Otherwise patch location ARADD with the address of the first AR11 and location ARVCT with the vector of the first AR11. If an unused address is not left after the last AR11, it is necessary to inhibit testing of more than one AR11 by patching 5ØØ3 into the 3$ location after location RBEG.

Refer to the diagnostic listing for detailed instructions, switch settings, etc. If an error occurs, the printout identifies the address of the failing register, so that the faulty AR11 in a system with multiple AR11's can be identified. Set front console SWØ9 = 1 to loop on the error and troubleshoot using the diagnostic listing, AR11 schematic and AR11 Circuit Descriptions.

4.2 AR11 Test II (analog) MAINDEC-11-DZARB-A

This diagnostic has three major uses - a calibration check (used with an EDC calibrated DC voltage source) for normal AR11 acceptance testing; on-going analog verification testing by users who do not have the BG5036 wraparound maintenance option; and

SIZE	CODE	NUMBER	REV
A	SP	AR11-Ø-6	

DEC FORM NO DEC 16-(381)-1022-N370
DRA 108

SHEET 4 OF 15

checkout of the scope control and scope when the AR11 is interfaced to an oscilloscope. These applications are described in detail in sections 4.4, 4.5 and 4.6 of the AR11 System Installation/Acceptance Procedure.

This diagnostic tests only one AR11 at a time. For an AR11 with address 77Ø4ØØ and vector 34Ø, no patches are needed. Otherwise, patch location ARADD with the address of the AR11 and location ARVCT with the vector. Program start location is 2ØØ. Refer to the diagnostic listing for detailed instructions.

4.3 AR11 Test III (wraparound) MAINDEC-11-DZARC-A

The wraparound diagnostic enables the AR11 to test itself, in conjunction with a G5036 wraparound module, which is connected to the AR11 through a BC08-R cable. The two D/A converters are combined in various manners using resistive dividers on the G5036 module and sent back into the A/D inputs. Consequently, both X and Y D/A's are tested by the A/D converter, and the A/D is tested by the D/A converters. Because the D/A's are divided down before going into the A/D, test resolution far better than 1 LSB is attained. In addition, the analog power supply levels (±14 Volts) are divided down and used as inputs, allowing test of the dc-to-dc converter; the four scope control logic outputs (ERASE L, NON-STORE L, CHØ2 L, and WRITE-THRU L) are used as inputs, allowing parametric tests of their high and low output levels; the CHØ2 L output

is fed back into the ERASE RET input, allowing test of the storage scope erase return handshaking logic; and the scope INTENSIFY output is fed back into the A/D external start input, allowing tests of both functions. Since all A/D input channels are used (at different input voltage levels), the wraparound module also provides a complete functional check on the A/D input multiplexer. Use of the various A/D channels by the wraparound test is as follows:

CHØ: Switchable between "Ø", a hard ground used in the wraparound program, and "E", a split lug useful for connecting an (EDC) calibrated DC voltage source.

CH1: Ground through 100K resistor, used for bias current test.

CH2: +5 VHQ power, divided down to +1 Volt nominal.

CH3: Positive analog supply, divided down to +2.5 Volts nominal.

CH4: Negative analog supply, divided down to -2.5 Volts nominal.

CH5: Coarse X and fine Y, Voltage ½X + 1/100Y, Code X + 1/50Y.

CH6: Coarse Y and fine X, Voltage ½Y + 1/100X, Code Y + 1/50X.

CH7: Fine Y, Voltage 1/100Y, Code 1/50Y

CH1Ø: Fine X, Voltage 1/100X, Code 1/50X

CH11: DirectX

CH12: DirectY

CH13: ERASE L

CH14: WRITE-THRU L

CH15: NON-STORE L

CH16: CHANNEL Ø2 L

CH17: +5 VHQ power, divided down to +4 Volts nominal.

Using the above inputs, the wraparound diagnostic MAINDEC-11-DZARC-A test the following:

a) Scope intensify pulse, external A/D start

b) Storage scope handshaking logic - Erase return, etc.

c) Scope control output logic high and low levels

d) Analog power supply levels

e) Functional check on all 16 channels of A/D input

f) A/D input bias current

g) Calibration of X D/A vs. A/D, Y D/A vs. A/D

h) Linearity of X D/A vs. A/D, Y D/A vs. A/D

i) Differential Linearity of A/D, X D/A, Y D/A

j) A/D inter-channel settling, plus full-scale and minus full-scale

k) Noise levels - rms and peak - A/D bipolar, A/D unipolar, X D/A, Y D/A

l) Offset - A/D bipolar, A/D unipolar, X D/A, Y D/A

In each of the above tests, the numerical results are compared to spec limits, and if everything passes, "END PASS" is printed out. A failure results in a corresponding error printout. Numerical results can be printed out by setting front console SW12 = 1.

The wraparound diagnostic is set up to automatically test multiple AR11's installed in a system, provided that the following

conditions are met: first (or only) AR11 address 77Ø4ØØ, vector 34Ø; additional AR11's 2Ø higher and sequential, e.g. 77Ø42Ø and 36Ø, 77Ø44Ø and 4ØØ, etc.; address which is 2Ø higher than the last AR11 address must be unused, e.g. 77Ø42Ø in system with one AR11, 77Ø46Ø in system with three AR11's. Otherwise, patch location ARADD with the address of the first AR11 and location ARVCT with the vector of the first AR11. If an unused address is not left after the last AR11, inhibit testing of more than one AR11 by patching 5ØØ3 into the 3$ location after location RBEG.

When running the wraparound program, each AR11 in the system must have a G5036 wraparound module installed. *Important Note: The BC08-R cable should be connected "upside-down" at the G5036 end, i.e. A to VV rather than A to A.

4.4 DEC/X11 Module MAINDEC-11-DXARA-A

The DEC/X11 module operates with or without the G5036 wraparound module installed. The program tests for the presence or absence of the G5036 and selects the proper routine accordingly.

If the G5036 module is available, it should be installed. In this case, the AR11 DEC/X11 exerciser uses wraparound techniques to measure (and compare to spec limits) rms and peak noise levels on A/D and both D/A's. All A/D conversions are started on clock overflow after a random number has been loaded into the clock preset register. Since the system is being exercised in the background

at the time of A/D conversion, true worst case noise levels are measured, under conditions of full system interaction. If an error is detected (any of the noise levels exceeds its spec limit), the program measures average value and peak-to-peak spread on the +5 VHQ and ±14 V power supplies, and reports these along with the error message.

If the exerciser senses that the G5036 module is not present, it executes a routine which takes conversions on each of the 16 channels, and displays them on the screen of the scope driven by the AR11. Each channel is displayed in turn for about three seconds.

5.0 AR11 TEST POINTS

The following test points are available on the AR11 module for troubleshooting purposes:

TPC: "Clock" - a 1 MHz TTL square wave output from the clock oscillator circuit. If this point is wrong, all bets are off, so that this is a good "quick look" first check for any AR11 problem.

TPG: "Logic Ground" - use for scope ground when checking AR11 logic signals. Scope should be floating to avoid ground loops.

TPHQ: "High Quality Ground" - use for scope ground when looking at AR11 analog signals. Scope should be floating to avoid ground loops.

TP+: "+14 VHQ" - positive analog supply.

TP-: "-14 VHQ" - negative analog supply. If TP+ and TP- are less

than ±13 Volts, analog problems may occur. The ±14 V levels should be checked first when verifying an analog problem.

TPPD: "Power Driver"- the power square-wave drive used in the dc-to-dc converter. This point is a good "quick look" first check for any ±14V power supply problem.

TPØ, TP1: Used for "all Ø's" and "all 1's" jumpers. See section 6.4 below.

TPSH: Sample-and-Hold output - tracks the selscted analog input signal +.8 Volts (unipolar) and +3.3 Volts (bipolar).

TPA: "A/D Approximation" - tracks the selected analog input signal during "sample", and zeroes in on ground in a series of decreasing plus and minus 2-microsecond steps during "hold".

TPE: "Enable A/D" - useful for external scope trigger to synchronize scope presentation to A/D conversion when looking at TPA.

6.0 TROUBLESHOOTING

6.1 Troubleshooting Flow

It will be useful to follow the flow of figure 1 below in troubleshooting an AR11. All troubleshooting of logic and dc-to-dc converter power supply should be done with reference to the AR11 schematics and AR11 Circuit Descriptions. Test points which are useful at the various points in the flow chart are indicated on the flow chart.

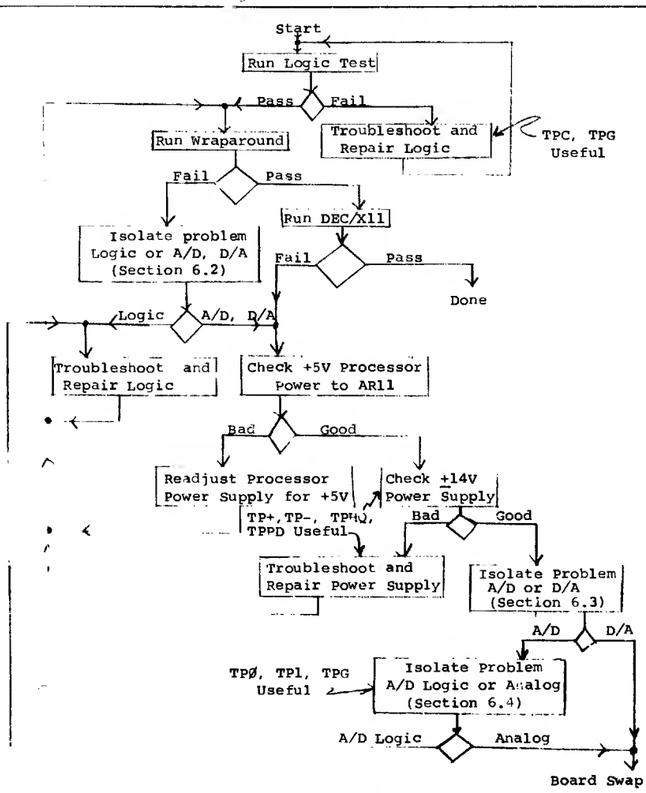


Figure 1: AR11 Troubleshooting Flow

6.2 Wraparound Problem - Logic on A/D, D/A?

Most problems uncovered by the wraparound program are in the A/D and D/A sections. The following logic problems, which can be fixed in FA & T or in the field, may be uncovered by the wraparound program:

6.2.1 "External A/D Start Failed" - The problem is with either the external A/D start logic or the scope intensify output pulse.

6.2.2 "VC Status Register in Error" - The problem is with either the erase flip-flop, erase return circuitry, or the CHANNEL Ø2 L output signal.

6.2.3 "VC Logic Signal High Output Too Low" and "VC Logic Signal Low Output Too High" - The problem is with the logic level of one of the four scope control logic outputs.

6.3 A/D or D/A?

In most cases, it will be obvious from the error message, error PC, and diagnostic listing comment field exactly where a given problem is - A/D, X D/A or Y D/A. For example the error message may identify a problem as "D/A differential linearity" or A/D inter-channel settling". In other cases, the error message may not identify the culprit, e.g. "Noise level exceeded limit" and it is necessary to refer to the comment field at the location in the error PC to identify the problem, e.g. "A/D bipolar rms

noise" or "X D/A peak noise".

The problem arises when a functional failure occurs in either the A/D or one of the D/A's (as opposed to some analog characteristic slightly exceeding its spec limit). In this case, multiple errors are printed out and it's not obvious whether the problem is in the A/D or one of the D/A's. The following table should aid in determining whether the failed device is A/D, X D/A, or Y D/A. Each of the wraparound tests uses some combination of A/D and D/A's. Those devices with an "X" are used in the indicated test.

TEST	A/D	X D/A	Y D/A
1			
2			
3	X		
4	X		
5	X		
6	X		
7	X		
10	X		
11	X		
12	X		
13	X		
14	X		
15	X		
16	X		
17	X		
20	X		
21	X		
22	X		
23	X		
24	X	X	X
25	X	X	X
26	X	X	X
27	X	X	X
30	X	X	X
31	X		X
32	X		X
33	X		X

34	X		X
35	X	X	X
36	X	X	X
37	X	X	X
40	X	X	X
41	X		X
42	X		X
43	X		X
44	X		X
45	X	X	X
46	X	X	X
47	X	X	
50	X		X
51	X	X	X
52	X	X	X
53			

In those cases, where it is impossible to determine from the above table whether it is the A/D or one of the D/A's which has failed, the individual Test II analog diagnostics should be run. If the AR11 is interfaced to a scope, Test II (B) will display a series of "pictures" which verify X and Y D/A operation.

If the "pictures" are good, the A/D can be assumed bad by process of elimination. This can be verified using Test II (C), the calibration test, and observing the output on the scope screen. If the AR11 is not interfaced to a scope, it is necessary to run Test II (C), the calibration test, and set front console SW10 = 1 to force printout of the converted value.

6.4 A/D Logic or Analog?

Once it has been determined that the A/D converter is non-functional, it is necessary to know whether the problem is in the

A/D successive approximation logic (which may be repaired) or in the A/D analog circuitry (which necessitates board swapping). This can be done with the "all Ø's" and "all 1's" jumpers. Jumpering TPØ to TPG bypasses the analog circuitry and simulates that output from the analog circuitry which results in a ØØØØ conversion. Jumpering TP1 to TPG bypasses the analog circuitry and results in a 1777 conversion. These numbers should be monitored using Test II (C), the calibration test. If ØØØØ and 1777 conversions do not result, the problem is in the A/D successive approximation logic. If ØØØØ and 1777 conversions do result, the problem is in the A/D analog circuitry.

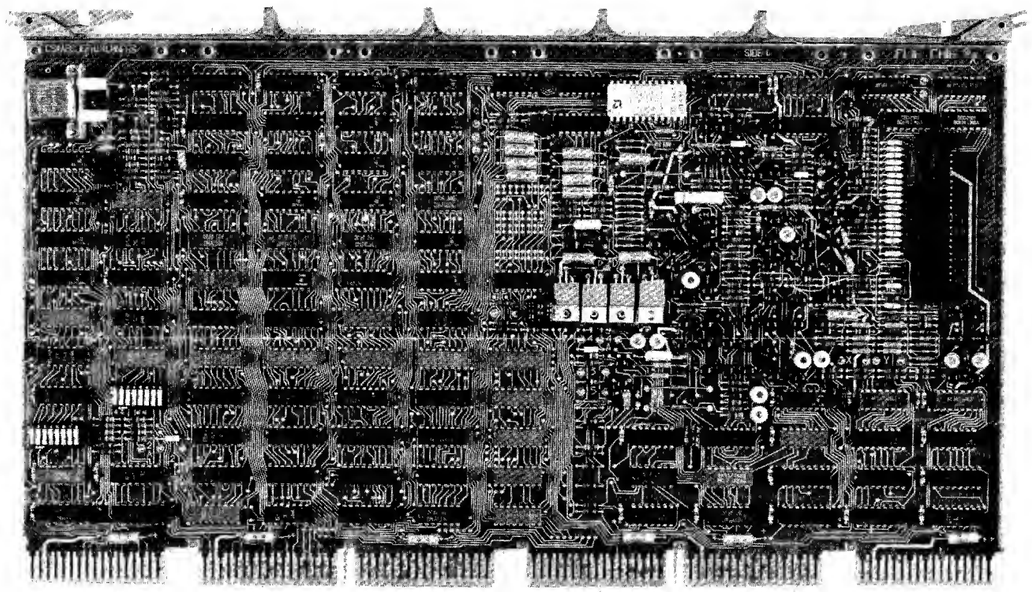
DIGITAL EQUIPMENT CORPORATION

LABORATORY AND SCIENTIFIC OPTION BULLETIN

pdp11

MAY 1975

AR11, Analog Real-Time Module



FEATURES

- Low Cost
- Compact
- Convenient interfacing and mounting
- Capabilities include:
  A/D converter—auto zeroing technique (patent pending)
  16-channel multiplexer, with sample and hold
  Programmable clock
  Scope display control with 2 D/A converters
  UNIBUS interface logic

DESCRIPTION

The AR11 is a compact analog real-time subsystem for use with the PDP-11 family of computers. Included in the subsystem are a 10-bit analog/digital converter, two 10-bit digital/analog converters, a crystal controlled clock, scope control, a 16-channel multiplexer, and a sample and hold circuit. Operation and selection of functions is under software control. Programming is subset-compatible with the LPS11, Laboratory Peripheral System, which is a more comprehensive analog processing system. The LPS11 is used for the larger and more demanding laboratory applications.

A/D Converter System

The 10-bit A/D Converter samples analog data at specified rates and allows the program to store the equivalent digital value for subsequent processing. Sample and hold circuitry ensures accurate conversions, even on rapidly changing signals, by holding the input voltage constant until the process is completed. The maximum throughput rate for a single channel is approximately 35 kHz. A 16-channel single-ended multiplexer is included. The input voltage range is program selectable for unipolar (0V to +5V), or bipolar (−2.5V to +2.5V) operation.

Display Control

The display control displays data in the form of a 1024 by 1024 dot array. Under program control, a bright dot may be produced at any point in this array. A series of these dots may be programmed to produce graphical output. The display control is primarily used with DIGITAL's VR14 display. However, it has the capabilities to operate with the Tektronix 602 and 604 display scopes and the 603, 611, and 613 storage scopes. It can also drive an X-Y analog recorder. The display control offers four program-controlled modes in which the scope can intensify a point. There are two 10-bit D/A converters with either a ±5V or a ±0.5V full scale output and all the necessary circuitry for scope control.

Programmable Clock

The programmable clock offers several methods for accurately measuring and counting time intervals or events. It can be used to synchronize the central processor to external events, count external events, measure intervals of time between events, or provide interrupts at programmable intervals. It can be used to start the A/D converter at predetermined intervals or from an external logic input.

The clock operates in one of two program modes: single interval or repeated interval. There are seven programmable frequencies: 1 MHz to 100 Hz, an external input, and an auxiliary input (on the backplane wiring).

An 8-bit counter can be preset for a number of time pulses or events to occur before an interrupt (or A/D counter start) is initiated. This counter can be read from the processor at any time to determine timing status.

PACKAGING

The complete AR11 subsystem electronics are contained on one single hex module that can mount in either of the two center slots of a DD11-B system unit, or within the CPU mainframe assembly. All external connections are made via a Berg connector (supplied with mating plug) which is mounted on an outside corner of the module.

Two types of cables are optionally available, BC11L-20 and BC08-R. The BC11L-20 is a 20-foot cable with a Berg connector on one end, open on the other end. The BC08-R is a Berg-to-Berg cable which connects the AR11 to the H322 Signal Panel, a general-purpose distribution panel with screw terminals. Signals from one or more of the user's devices may be brought into the screw terminals on the panel.

No external analog supply voltages are required. A unique DC to DC converter without transformer uses the +5V logic power to generate the high-quality positive and negative voltages needed by the AR11.

PROGRAMMING

There are 8 registers used for control and data. The address of the first register is selectable in increments of 20, between 770 000 and 777 760. With a starting address of 770 400, the arrangement is:

Register	*Address*
A/D Status	770 400
A/D Buffer	770 402
Clock Status	770 404
Clock Buffer	770 406
Display Status	770 410
X Buffer	770 412
Y Buffer	770 414
Clock Counter	770 416

There are three interrupt vectors, with the address of the first address vector selectable in increments of 20. If the first vector is at 300, the arrangement is:

Vector	*Address*	*Priority Level*
A/D	300	BR6
Clock	304	BR6
Scope Control	310	BR4

SPECIFICATIONS

A/D Converter System

Input voltage range:	0 to +5V, or −2.5V to +2.5V, program selectable
Resolution:	10 bits (1 part in 1024)
Accuracy at 25°C:	±0.1% of full scale
Linearity:	½ LSB
Conversion time:	22 to 24 μsec
Number of input channels:	16
Input impedance:	10M ohms, min.
Settling time; (MUX plus S & H):	8 μsec, max. (5-volt step)

Scope Control

D/A Output voltage range:	−5V to +5V, or −0.5V to +0.5V, jumper selectable (2 D/A's)
Resolution:	10 bits
Accuracy at 25°C:	±0.1% of 10V full scale, or ±2% of 1V full scale
Scopes controlled:	VR14, Tektronix scopes including storage scopes

Programmable Clock

Clock rates:	1MHz, 100 kHz, 10 kHz, 1 kHz, 100 Hz (crystal controlled); external logic input; auxiliary frequency input
Operating modes:	single interval, repeated interval
Counter size:	8 bits
Preset register size:	8 bits
Accuracy:	±0.005%
External input:	TTL logic
Aux. freq. input:	TTL logic, accessible on backplane

Mechanical

Mounting:	1 hex module slot
User Interface:	Berg connector on the module

Power

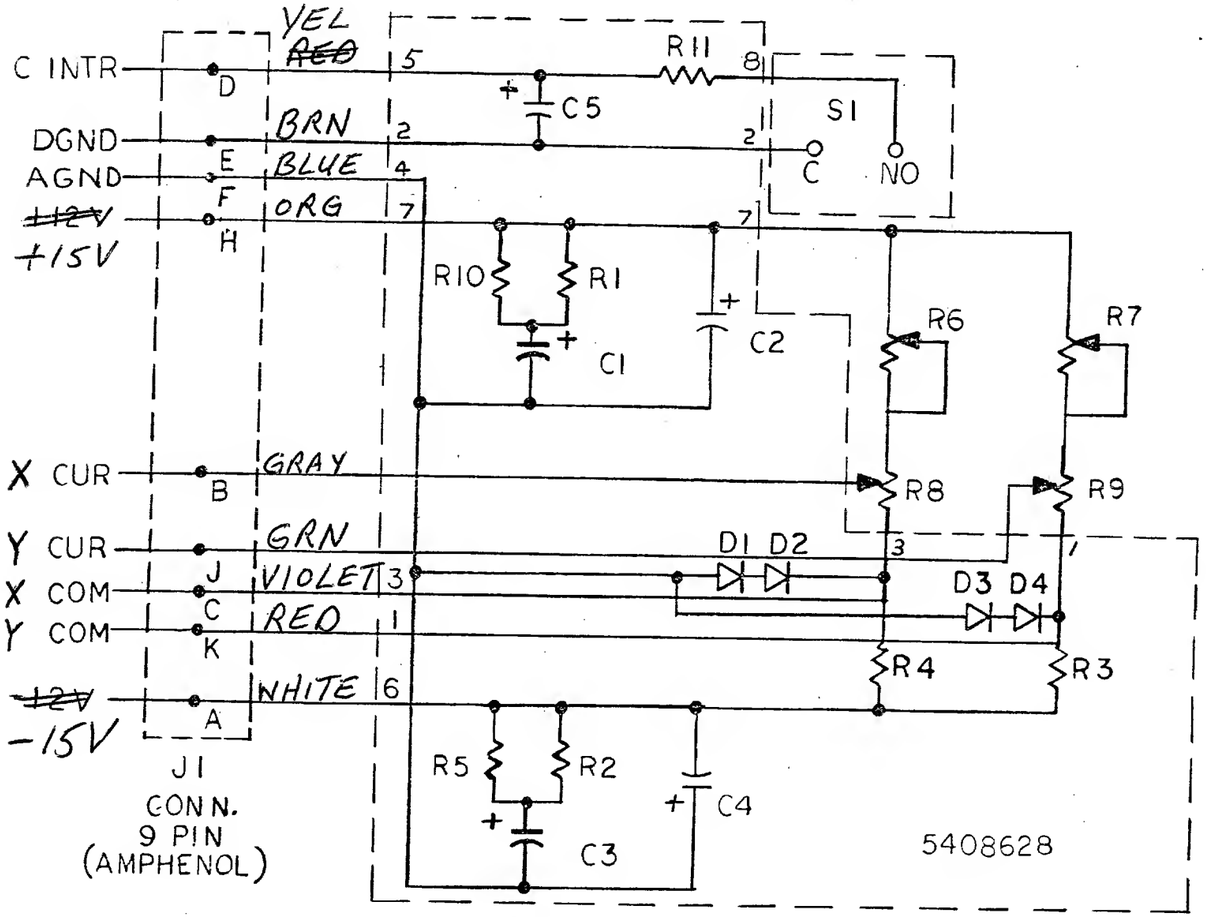
4A at +5V

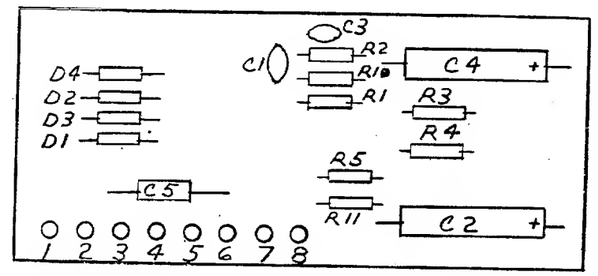
Environment

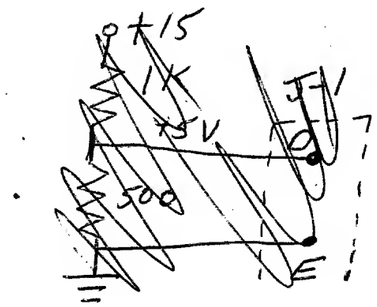
Operating temperature:	15°C to 52°C, system ambient
Relative humidity:	10% to 90%

digital

SIZE B | CODE CS | NUMBER H3Ø6-Ø-1 | REV D

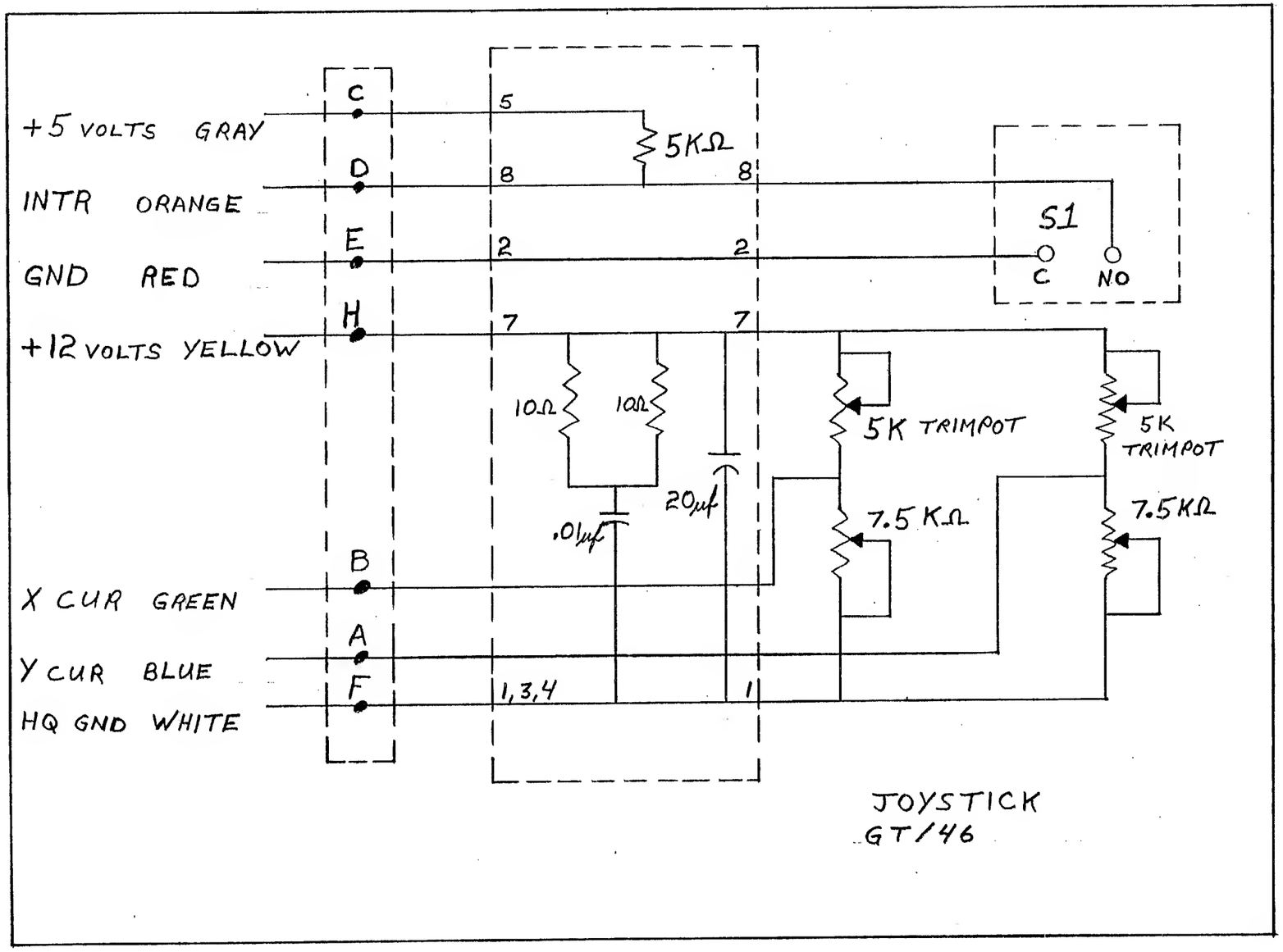






C INTR = A/D CH2
X CUR = A/D CH1
Y CUR = A/D CHØ

D1, D2, D3, D4	D664 DIODE	1100114
C5	CAPACITOR 6.8 μf	10053CE
S1	SWITCH E-63-00A (CHERRY)	1209782
C2, C4	CAPACITOR 20μf	1002839
R1, R2, R5, R10, R11	RESISTOR 10Ω	1301317
C1, C3	CAPACITOR .01μf	1001610
R3, R4	RESISTOR 3.3 K	1300439
R8, R9	RESISTOR 2.5K	1309306


C
D
E
H
B
A
F
+5 VOLTS GRAY
INTR ORANGE
GND RED
+12 VOLTS YELLOW
X CUR GREEN
Y CUR BLUE
HQ GND WHITE
5
8
2
7
1,3,4
1
5KΩ
10Ω
10Ω
.01μf
20μf
5K TRIMPOT
5K TRIMPOT
7.5 KΩ
7.5KΩ
S1
C
NO
JOYSTICK
GT/46